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1. WO2023220537A1 (and Family Patents: KR20250020455A, CN119678130A, GB2634424A, JP2024566885, US18864662, CA3253057, SG11202407900T, IN202417097720)

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PATENT SNAPSHOT

- ## ABOUT INVENTION

THE INVENTION DESCRIBED IN 'WO2023220537A1', TITLED 'SIMPLE AND LINEAR FAST ADDER', DESCRIBES A FAST ADDER DESIGNED FOR USE WITHIN AN ARITHMETIC LOGIC UNIT (ALU) BY INTRODUCING A FUNDAMENTALLY NOVEL ARCHITECTURE BASED ON A FINITE STATE MACHINE MODEL OF ADDITION. THE SLFA IS ENGINEERED FROM THE GROUND UP AND IS INHERENTLY COMPATIBLE WITH A COMPUTE-IN-MEMORY (CIM) ARCHITECTURE AT THE ALGORITHMIC LEVEL.

ITS CORE IS A N-BIT ADDER UNIT CONSTRUCTED FROM N-MANY IDENTICAL SUBUNITS CONNECTED IN SERIES, EACH SUBUNIT CONSISTING OF ONE AND GATE AND ONE XOR GATE, INTEGRATED WITH A TWO-BIT REGISTER. THE DESIGN ACHIEVES LOGARITHMIC DELAY FOR HIGH-SPEED COMPUTATION WHILE MAINTAINING A LINEAR AREA COMPLEXITY AND CONSTANT GATE DEPTH, ENSURING PREDICTABLE, LOW POWER DISSIPATION REGARDLESS OF INPUT SIZE.

A KEY INNOVATION IS THE NATURAL ONE-TO-ONE CORRESPONDENCE BETWEEN MEMORY AND LOGIC. THE ADDER'S FINITE STATE MACHINE OPERATES THROUGH LOCALIZED INTERACTIONS BETWEEN ADJACENT MEMORY REGISTERS AND LOGIC GATES, ELIMINATING THE NEED FOR COMPLEX, LONG-DISTANCE CARRY CHAINS. THIS LOCALITY ALLOWS THE MEMORY CELLS AND LOGIC TRANSISTORS TO BE CO-LOCATED IN A DENSE, REGULAR GRID, DIRECTLY MITIGATING THE VON NEUMANN BOTTLENECK BY MINIMIZING DATA MOVEMENT.

UNLIKE OTHER CIM PROPOSALS, OUR IP ARCHITECTURE DOES NOT REQUIRE HUGE R&D INVESTMENT INTO FINDING NEW TRANSISTOR AND MEMORY TYPES, NEW MANUFACTURING PROCESSES, OR OVERLY COMPLICATED NICHE DESIGNS. OUR SIMPLE LINEAR FAST ADDER (SLFA) NATURALLY EMBEDS COMPUTATION WITHIN THE MEMORY FABRIC, USING ONLY STANDARD CMOS LOGIC GATES AND EDGE-TRIGGERED REGISTERS, BYPASSING THE ENTIRE RESEARCH

PROCESS FOR NEW NON-STANDARD TRANSISTORS AND MEMORY CELLS. IT OFFERS A PRACTICAL, MANUFACTURABLE PATH TO CIM BY COMBINING MEMORY REGISTERS AND COMPUTATIONAL LOGIC INTO A REGULAR GRID—ENABLING BITWISE OPERATIONS, ROTATIONS, AND ADDITION TO BE EXECUTED IN-SITU WITHOUT COSTLY DATA MOVEMENT.

- ❖ LOW-POWER, LOW-COST ARCHITECTURE
  - REGULAR, DENSE PACKING. MORE CORES PER WAFER!
- ❖ WIDE RANGE OF APPLICATIONS
  - FUNDAMENTAL SOLUTION TO A FUNDAMENTAL PROBLEM.
  - IMPACT ON SEVERAL KEY INDUSTRIES.
- ❖ REGULAR GRID DESIGN AND SCALABLE BIT CAPACITY.
  - FEWER METAL LAYERS NEEDED AND BETTER THERMAL PROFILE (DISTRIBUTED HEAT).
  - REGULAR PATTERN WITH PREDICTABLE ROUTING AND CONGESTION. EASY TO TEST.
- ❖ IN-SITU PROCESSING (SUPER-FAST AND ENERGY-EFFICIENT)
  - THE DISTANCE BETWEEN THE MEMORY AND ITS ASSOCIATED LOGIC IS REDUCED TO THE LENGTH OF A WIRE BETWEEN A FLIP-FLOP AND ITS NEIGHBOR GATE—ESSENTIALLY ZERO. WIRE CAPACITANCE IS AN IMPORTANT ENERGY CONSUMER.
  - HIGHER POSSIBLE CLOCK SPEEDS (SHORTER CRITICAL PATHS AND GATE DEPTH).
- ❖ BASED ON STANDARD CMOS MEMORY AND TRANSISTOR TECHNOLOGY
  - CHEAPER MASKS.
  - FASTER TIME-TO-MARKET.

THIS MAKES THE SLFA A TRANSFORMATIVE SOLUTION NOT ONLY FOR HIGH-SPEED, LOW-POWER ARITHMETIC IN TRADITIONAL CPUS, DSPS, AND ASICS BUT ALSO AS A FUNDAMENTAL BUILDING BLOCK FOR EFFICIENT, SCALABLE COMPUTE-IN-MEMORY SYSTEMS, AI ACCELERATORS, AND NEXT-GENERATION HARDWARE.

BIBLIOGRAPHY

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i. WO2023220537A1 (and Family Patents: KR20250020455A, GB2634424A, CN119678130A, JP2024566885, US18864662, CA3253057, SG11202407900T, IN202417097720)

TITLE:	Simple and linear fast adder
PATENT NUMBER:	N/A
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PRIORITY NUMBER:	US202263340865P
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IPC CLASSES	G06F7/505, G06F7/575, G06F7/42, G06F7/556
Assignee Orig.	N/A

Abstract:

Disclosed herein is a fast adder design based on a novel axiomatization of mathematics, of natural and real numbers, by the author. Addition is a Finite State Machine that, on an average, takes $\log_2 n$ iterations to calculate a n-bit addition. Further, for the proposed fast adder, the probability of a n-bit addition taking $k \leq n$ iterations to complete, is equal to the probability of k consecutive heads in n fair coin tosses. The circuitry is linear and simple, in the sense that adding bits to the inputs does not complicate the circuit topology. The growth is linear, and the instruction set is constant, and hardware based.

OTHER FAMILY PATENTS:

Title	Patent no.	Application no.	Priority Date	Validity Up to
A simple linear fast adder	JP2025522231A	JP2025522231A	11-May-2022	N/A
Simple linear fast adder	CN119678130A	CN119678130A	11-May-2022	N/A
Simple linear high-speed adder	KR20250020455A	KR20250020455A	11-May-2022	N/A
Simple and linear fast adder	GB2634424A	GB2634424A	11-May-2022	N/A
Simple and linear fast adder	CA3253057	CA3253057	11-May-2022	N/A
Simple and linear fast adder	SG11202407900T	SG11202407900T	11-May-2022	N/A
Simple and linear fast adder	US18864662	US18864662	11-May-2022	N/A
Simple and linear fast adder	IN202417097720	IN202417097720	11-May-2022	N/A

TECHNOLOGY ANALYSIS

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1. TECHNOLOGY OVERVIEW

This report highlights a novel arithmetic architecture based on a Finite State Machine (FSM) model of addition, implemented as a Simple and Linear Fast Adder (SLFA). The invention introduces a highly efficient four-bit adder element constructed from a combination of four AND gates, four XOR gates, and four sets of two-bit registers. The adder is engineered with a linear area and gate complexity, ensuring a minimal and scalable silicon footprint as bit-width increases.

Unlike traditional carry-propagate or parallel-prefix adders, the SLFA achieves logarithmic average delay while maintaining a constant gate depth, simple and regular connections, and linearly scalable topology, resulting in predictable, low power dissipation. All these factors translate into an optimally efficient (in time, energy, area and gate count) arithmetic core with full bit scalability, little R+D overhead, and standard manufacturing processes. The final and most important characteristic of this circuit, is that this design places the memory and logic gates next to each other in a natural one-to-one correspondence, making it a CIM architecture (Memory/ALU bandwidth is eliminated) because of this natural proximity between the memory and the logical gates. The FSM operates through localized interactions. This co-location of storage and computation eliminates long-distance data carries and minimizes energy-intensive data movement, directly addressing the Von Neumann bottleneck. We have solved the problem not at the physical (material) level, but at the algorithmic (mathematical) level. This design directly addresses the On-Chip Memory-Wall with a true CIM architecture using standard CMOS memory cells (edge-triggered flip-flops) by redefining the very algorithm for addition. The input data is the initial state of the memory registers, and the state evolves in place through local interactions. The computation is carried out as the data flows through this regular grid of memory and gates. Instead of trying to make memory cells perform logic (like ReRAM, MRAM or FeFET), we designed an adder where the fundamental topology embeds memory and logic in a one-to-one, adjacent manner. While others are trying to make memory compute, we're making computation circuits more memory-like. We essentially describe addition as a cellular automaton where each cell contains:

- A small memory (2-bit register)
- Two fundamental logic gates (AND, XOR)
- Local connections to neighbors

This makes the SLFA uniquely valuable not only for performance-critical and power-sensitive applications like embedded processors, ASICs, and SoCs but also as a foundational core for next-generation CIM systems and AI accelerators. The design can be commercialized as a reusable semiconductor IP core, offering a superior balance of speed, area efficiency, and power consumption. It can function as a standalone arithmetic block or be tiled into larger arrays for parallel multi-input addition and matrix multiplication.

The memory element we require to implement our proposed CIM architecture is not a research problem; it's a mature component. The innovation is in the algorithm and resulting topology that turn these ordinary components into an extraordinary, bottleneck-breaking arithmetic circuit. The memory elements are not "special compute cells"; they are standard edge-triggered D-type flip-flops (DFF). We bypass the need for new materials or exotic transistor types, and non-standard fab processes. Some of the biggest advantages in using DFF's are:

- The fundamental building block of all digital design.
- Perfectly regular, dense, and have decades of optimization in speed, power, and area.
- Natively support the double-edge-triggered (read-on-rise/write-on-fall) operation we require. DFFs are the easiest on-chip memory elements to manufacture.
- They are part of every standard cell library.

Overall, this innovation meets the growing demand for compact, high-performance, and energy-efficient computing primitives across a wide range of applications, from consumer IoT devices to data center AI hardware and transformative Compute-in-Memory architectures.

2. TECHNOLOGY DIVISION (TYPES)

The technology division in the Simple linear fast adder market is typically divided into several key types, each designed to address specific operational needs:

Logic Integrated Circuit (ICs)	*Our linear fast adder serves as a core logic circuit, making it an essential building block in ALUs, encoders, decoders, and other digital ICs. With its predictable low-power performance and logarithmic delay, it provides a scalable solution for a wide range of logic IC applications.*
Microprocessor (Processor ICs)	*Designed specifically for ALUs, the adder directly enhances CPU, microcontroller, and DSP architectures. By reducing power dissipation while maintaining high speed, it improves overall processor efficiency a critical factor in today's performance-driven computing markets.*
Application Specific Integrated Circuit (ASICs)	*As a customizable logic block, our adder integrates seamlessly into ASIC designs for IoT, networking, AI acceleration, and mobile processors. Its energy-efficient architecture supports domain-specific optimization, aligning for tailored semiconductor solutions.*
FPGA & Programmable Logic Devices	*In FPGA platforms, where flexibilty and prototyping speed are crucial, our adder can be packaged as soft IP to accelrate arithmetic operations in configurable logic blocks. This capability positions it strongly within the FPGA and CPLD market.*
Data-Center Chips	*In the Data Centre Chip segment, where performance-per-watt is critical, our adder enhaces arithmetic throughput while maintaining constant power characteristics. This directly benefits workloads in AI, cloud, and big data by improving efficiency and scalability.*

3. TECHNOLOGY COMPARISON

The pursuit of computational efficiency has led the industry down several paths, each with significant trade-offs. While others are trying to solve the Von Neumann Bottleneck in the lab with new materials like MRAM or ReRAM, we've solved it at the algorithmic level. The Simple Linear Fast Adder (SLFA) we propose is the only solution that delivers the performance of parallel architectures with the scalability and manufacturability of linear designs, fully enabled to compute general arithmetic operations In-Memory. The FAU's core innovation is a mathematical and architectural breakthrough that enables Compute-In-Memory using standard CMOS cells and manufacturing processes. Our IP's value proposition is digital, precise, scalable, and immediately fabricable CIM using the industry's most mature and cost-effective memory element: the CMOS flip-flop. Once the GDSII prototype design files are complete, it can be manufactured in a CMOS logic process (TSMC, Intel, Samsung) immediately.

- ***Manufacturability**:* Can be built in any standard CMOS fab (TSMC, Samsung, Intel). The regular grid dramatically simplifies place-and-route, reduces layers, and boosts yield. With no dependency on exotic materials or processes, the design can be taped out in existing fabs in a fraction of the time required for complex, irregular layouts because everything is predictable and regular from design to testing and production.

- ***Performance**:* Logarithmic average time, constant power profile, and linear scalability.

- ***Targeted:*** There is an obvious memory-wall between the external memory units and a processor. This is the off-chip bottleneck. Most solutions addressing the memory-wall will focus on the off-chip bottleneck by placing memory subarrays and localized computing cores closer to each other. But there are also memory elements inside the processor called registers. The Arithmetic-Logic Unit is located in one region of the chip, while the registers are in a separate region of the chip. This separation constitutes the on-chip memory-wall. Some solutions to the on-chip memory-wall optimize cache and memory hierarchies (on-chip SRAM), shortening the distance to the computing engines (for example Near-Memory Computing implemented by Etched), but this is not a fully satisfying solution. We provide a fundamental solution to this on-chip bottleneck, the only real memory-wall remaining.

- ***Applicability**:* Other CIM solutions are not dependent on exotic materials but are niche designs used to accelerate very specific processes (again, Etched, Mythic AI and Neuroblade are just a few examples). Our SLFA is a universal building block for high-performance arithmetic cores that benefits any type of processor, and targets the massively parallel, arithmetic-heavy, and power-sensitive domains of Bitcoin mining, AI edge devices and DSP, among many others, because we address the most fundamental and commonly executed operation: Addition of multiple inputs.

- ***Functionality***: The SLFA can be generalized into a rectangular grid that performs addition of multiple inputs and can be scaled for area-efficient matrix multiplication.

Our design allows locality of memory and logic at the bit level. We don't just place a computing engine next to a memory subarray. Our addition algorithm embeds the computing logic in a one-to-one correspondence with the memory cells bit-by-bit. The result is a completely new architectural paradigm for extreme computational efficiency. This general-purpose adder eliminates data movement and can be generalized to a rectangular block that performs addition of multiple inputs and scaled to achieve area-efficient matrix multiplication.

This isn't just an incremental improvement - it's a complete rethinking of how computation logic and memory cells should be physically laid out on silicon. The result is an ASIC that redefines mining economics: more cores per wafer, significantly lower power consumption, and operational resilience through market cycles. While competitors chase incremental optimizations within the Von Neumann bottleneck, our SLFA-based grid erases that bottleneck altogether—delivering not just a better mining chip, but a new architectural paradigm for ultra-efficient, deterministic computation.

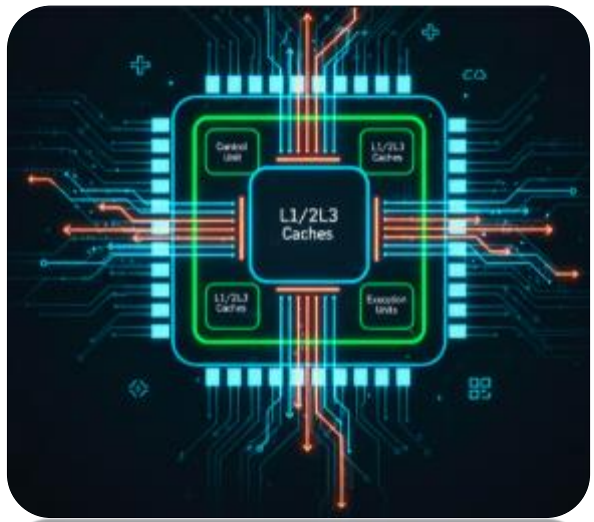
CIM Processors	A conceptual solution was proposed decades ago as an attempt to bypass the Von Neumann Bottleneck.
	Performs computations directly within the memory, offering transformative improvements in time performance and energy efficiency.
	Requirement of significant resources in research and development of new transistor and memory types. Involves new materials, new machines, new processes etc.
Fast Arithmetic Unit	Low-power, low-cost Simple and Linear Fast Adder that offers unparalleled efficiency and performance, with linearly scalable bit capacity.
	Area-Optimized Matrix Multiplication
	Flexible Configuration (Programmable Array)
	In-Situ Processing (Super-Fast and Energy Efficient) rectangular grid array in perfect rows and columns that executes fast multiplication and addition of multiple inputs.
	Based on Standard CMOS Memory and Transistor Technology and does not require research into expensive manufacturing processes.

4. APPLICATION OVERVIEW

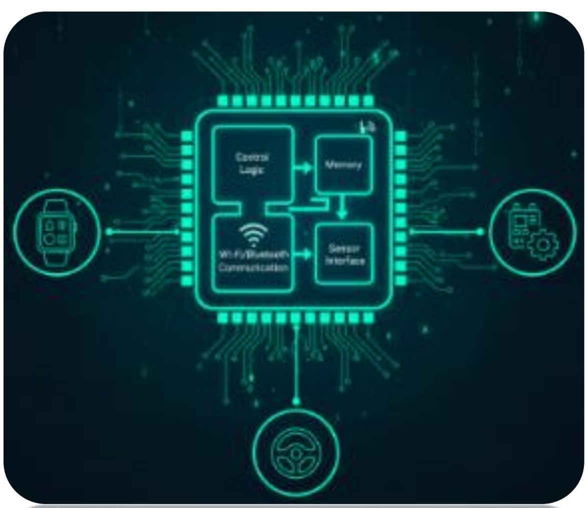
The application areas of the Simple and Linear Fast Adder span over a wide range of industries. The market is typically divided into several key types, each designed to address specific operational needs. Here's an overview of how these technologies are applied across various sectors:

A. Central Processing Unit (CPUs):

The CPU market is built on advanced arithmetic and logic circuits that enable faster execution and improved efficiency. High-performance adders, multipliers, and logic blocks are integrated into execution pipelines to reduce delay and manage power consumption. Growth is driven by demand in personal computing, servers, and mobile processors, with future development focused on heterogeneous compute architectures, advanced packaging & continued scaling.



B. Embedded System:

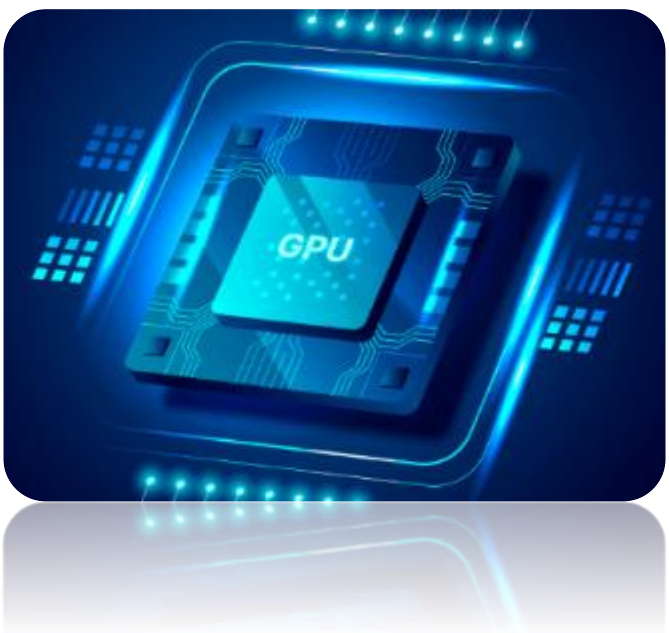


Embedded systems rely on compact, low-power chips that integrate sensors, communication modules, memory, and arithmetic units to support real-time control and monitoring. These systems are central to IoT, industrial automation, automotive electronics, and consumer devices. Market expansion is fueled by smart cities, healthcare monitoring, and autonomous technologies. Future developments include AI-enabled embedded processors & ultra-low-power architectures to deliver intelligence at the edge.

C. Digital Signal Processing (DSP):

Digital signal processors are optimized for repetitive arithmetic operations such as filtering, transforms, and compression, making them essential for telecommunications, multimedia, radar, and medical imaging. Their role in enabling real-time signal transformation continues to expand with the growth of 5G, high-resolution sensors, and edge AI. Development trends point toward domain-specific accelerators and AI-augmented DSPs that combine traditional signal processing with neural network capabilities.

D. Graphics Processing Units (GPUs) & AI accelerators:



GPUs and AI accelerators are designed around massively parallel arithmetic engines that support graphics rendering, machine learning, and scientific computation. These architectures enable efficient handling of large-scale, data-intensive workloads, making them indispensable for gaming, AI training, and data center applications. Market growth is supported by expanding AI adoption, real-time graphics in AR/VR, and HPC infrastructure.

E. Low-Power Computing & IOT Device

Low-power computing underpins the operation of battery-driven IoT devices, wearables, and edge nodes where energy efficiency is critical. Chips for this market integrate compact arithmetic units and control logic optimized for predictable power usage, extending device lifetimes without sacrificing responsiveness. Future advancements will include energy-harvesting systems, adaptive architectures for dynamic power scaling, and design methodologies that minimize leakage and thermal load.

F. Custom Hardware for Cryptography

Cryptography hardware incorporates specialized arithmetic and logic circuits to support modular arithmetic, encryption algorithms, and secure key storage. These secure components are widely deployed in payment systems, hardware security modules, and trusted platforms. Market growth is driven by rising cybersecurity needs, financial digitization, and demand for secure IoT deployments. Future development is expected in post-quantum cryptographic hardware, ultra-low-power secure processors, and integrated crypto accelerators for consumer and enterprise platforms.

G. Compute-in-memory

Compute-in-memory architectures integrate processing functions directly within memory arrays to reduce data movement, improve latency, and enhance energy efficiency. By embedding arithmetic operations into storage units, CIM addresses bottlenecks in data-intensive applications such as AI, analytics, and big data processing. The market is gaining momentum with research in non-volatile memory technologies like RRAM and MRAM, as well as 3D-stacked memory approaches.

H. High Performance Computing (HPC)

High-Performance Computing (HPC) provides immense computational capacity for complex simulations, scientific research, and data-intensive analytics. These systems leverage parallel processing to accelerate execution and optimize workload distribution. Key industries such as climate science, genomics, and finance rely on HPC for advanced problem-solving. The rise of AI and machine learning is intensifying demand for scalable HPC solutions. Ongoing improvements in processors, interconnects, and energy efficiency continue to propel the market.

MARKET ANALYSIS

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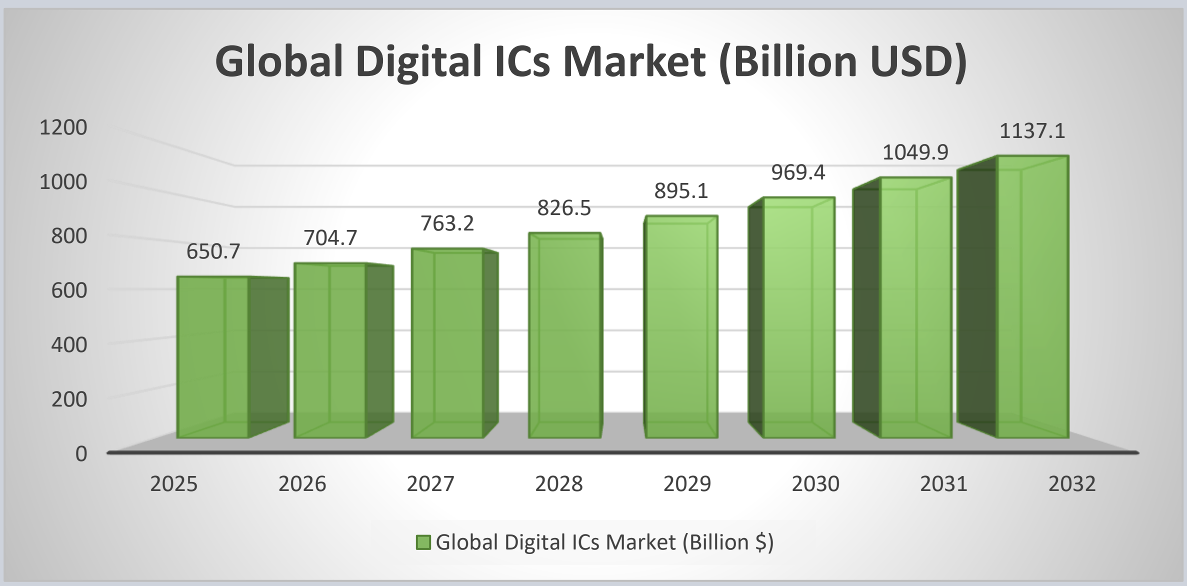
DIGITAL INTEGRATED CIRCUIT (ICs) OVERVIEW & GLOBAL MARKET

The Digital Integrated Circuit (ICs) market is rapidly emerging as one of the most transformative and high-growth sectors in the global economy. **At the core of these circuits are arithmetic functions, where adders serve as an integral component of processing and logic operations.**

Currently valued in the hundreds of billions of dollars, the digital integrated circuit (IC) market is expanding rapidly, driven by advances in technology and rising demand for consumer electronics like smartphones, laptops, and PCs. Increasing miniaturization of these devices has significantly propelled the digital IC sector, enabling higher performance in smaller, more efficient form factors.

The global Digital ICs market is estimated to be values at USD 650.7 billion in 2025 and is expected to reach USD 1137.1 billion by 2032, exhibiting a compound annual growth rate (CAGR) of 8.3 % from 2025 to 2032.

This remarkable growth of digital ICs market is fueled by booming consumer electronics, advances in automotive systems, and wider use of signal processing across industries. With the industries shifting toward higher speeds and lower power consumption, **advancements in adder design are becoming increasingly valuable, reinforcing their central role in driving digital IC performance and market growth.**



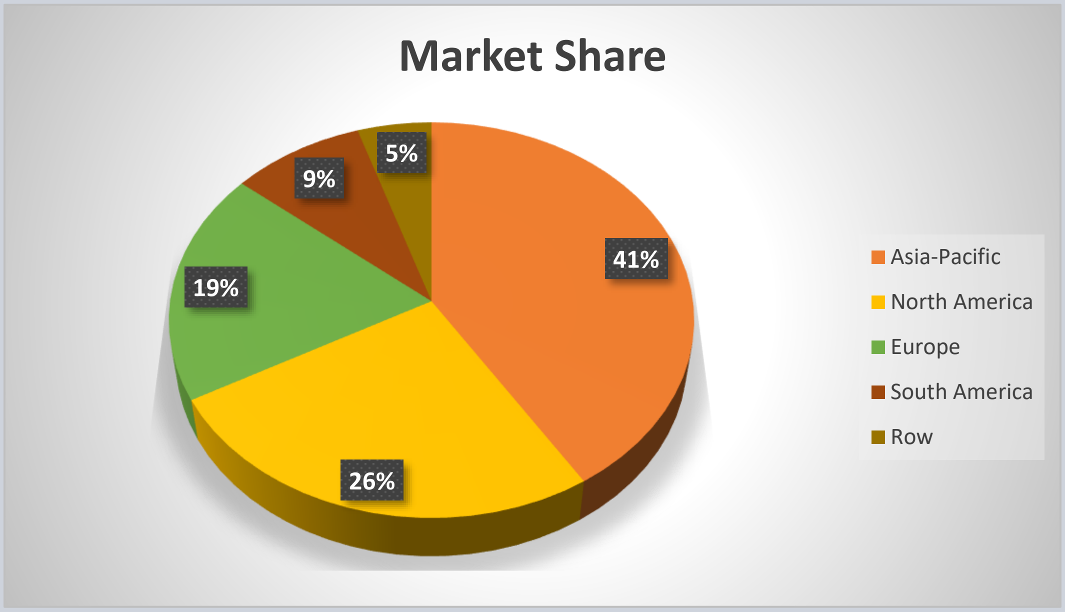
DIGITAL INTEGRATED CIRCUIT (ICs) REGION BASED MARKET

The global Digital Integrated Circuit (ICs) market is segmented into Asia Pacific, North America, Europe, South America and the Rest of the World, each showing unique growth drivers.

Asia Pacific dominates the global market with a leading share of 41%, followed by North America, which holds 26% of the market. Europe captures 19%, positioning it as the third-largest regional player. The remaining market share is distributed across the south America with 9% market and rest of world with 5% market. Together, these regions shape the overall dynamics of the global market.

Differences in regional valuations highlight diverse market dynamics and growth prospects, shaped by local industry needs and the pace of technology adoption.

Market players in the Digital Integrated Circuits industry are adopting diverse strategies to strengthen their position and meet the growing technical requirements of sectors such as consumer electronics, automotive, telecommunications, and healthcare. Notable players in the global Digital Integrated Circuit market includes Taiwan semiconductor, Samsung Corporation, Integrated Device Technology, Texas Instruments, ST Microelectronics, Analog Devices, Intel and Infineon Technologies.



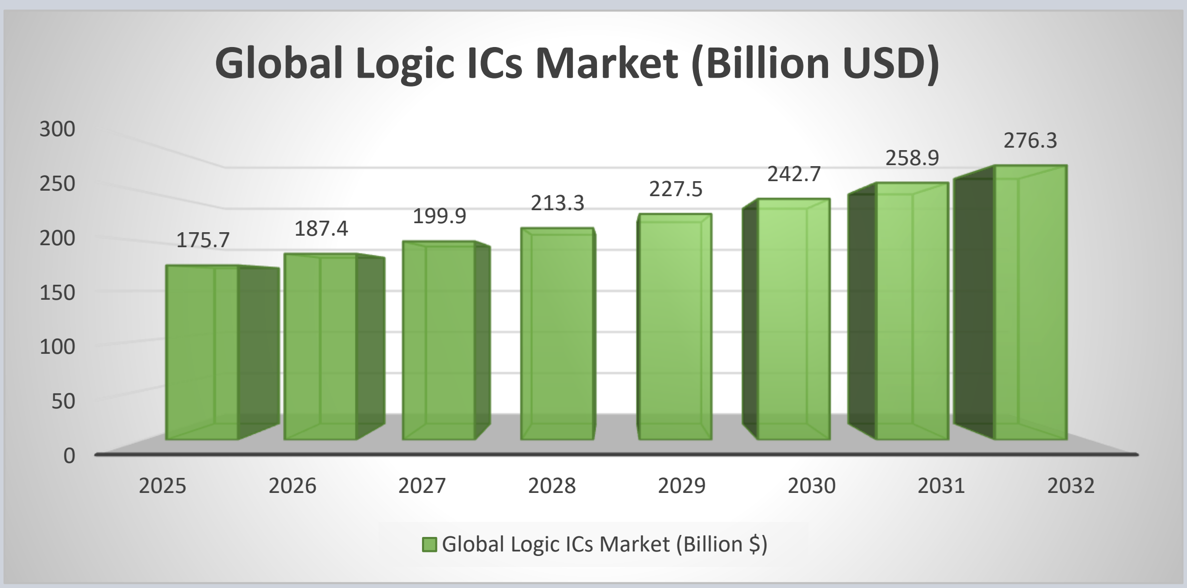
- **Logic Integrated Circuit (ICs) Market Overview**

The global logic integrated circuits market is witnessing steady growth, driven by the need for advanced computing, greater industrial automation, and the widening scope of consumer electronics applications.

The global Logic Integrated Circuit market was valued at USD 175.76 Billion by 2025. Looking further ahead, the market is expected to grow significantly, reaching an estimated USD 276.38 Billion by 2032. This growth reflects a robust compound annual growth rate (CAGR) of 6.68% during the period from 2025 to 2032.

The Logic Integrated Circuit (ICs) market forms the backbone of digital electronics, powering functions from simple logic operations to complex data processing. **Among these circuits, adders are a critical element, providing the arithmetic capability that underpins broader system performance.** Their efficiency and design directly impact the speed, reliability, and power profile of logic ICs, making them a key factor in meeting rising market demands.

As the need for high-performance, low-power devices grows, advanced adder architectures can significantly enhance the value and adoption of Logic Integrated Circuits (ICs) across industries.



- <u>Logic Integrated Circuit (ICs) Regional Market Analysis</u>

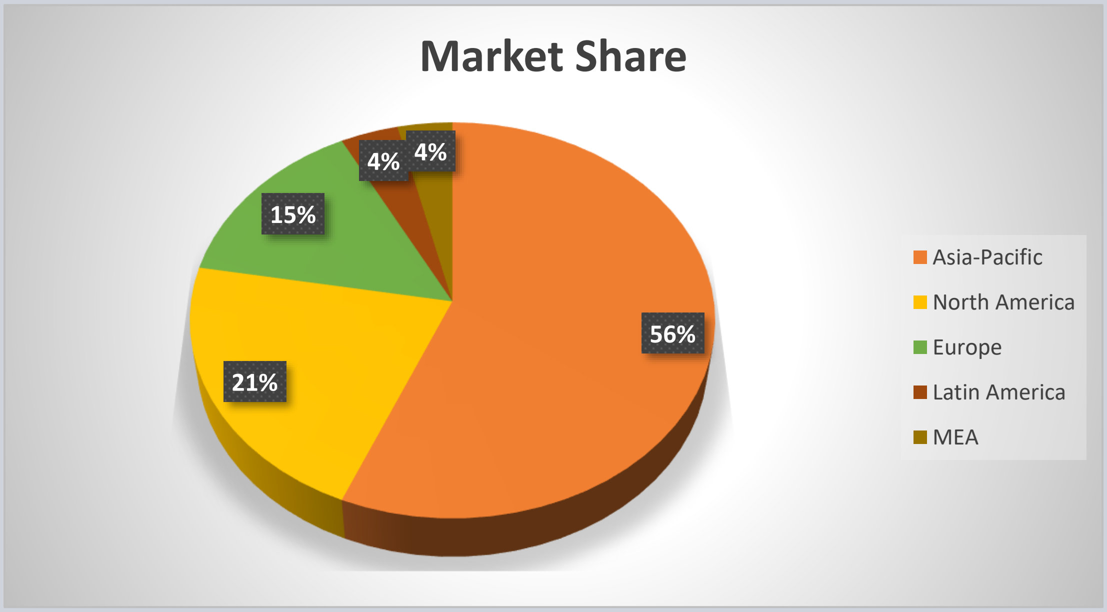
The global Logic Integrated Circuit (ICs) market is segmented into Asia Pacific, North America, Europe, Latin America and Middle East & Africa, each showing unique growth drivers.

Asia Pacific dominates the global market with a leading share of 56.3%, followed by North America, which holds 21.5% of the market. Europe captures 14.6%, positioning it as the third-largest regional player. The remaining market share is distributed across the Latin America with 3.9% market and rest of world with 3.7% market. Together, these regions shape the overall dynamics of the global market.

China leads Asia Pacific with large-scale manufacturing, government backing, and rising electronics demand, reinforced by investments in semiconductor self-reliance.

North America's logic IC market benefits from strong demand in electronics, automotive, and data centers, with the U.S. leading through advanced R&D, the CHIPS Act, and cutting-edge foundry capabilities. Europe's logic IC market grows steadily, driven by automotive electronics, industrial automation, and telecom, with Germany and France advancing adoption through EV innovation and advanced manufacturing.

In the Middle East & Africa, the UAE dominates through smart city initiatives, 5G expansion, and electronics demand. Latin America is led by Brazil, supported by consumer electronics, automotive growth, and pro-semiconductor policies.



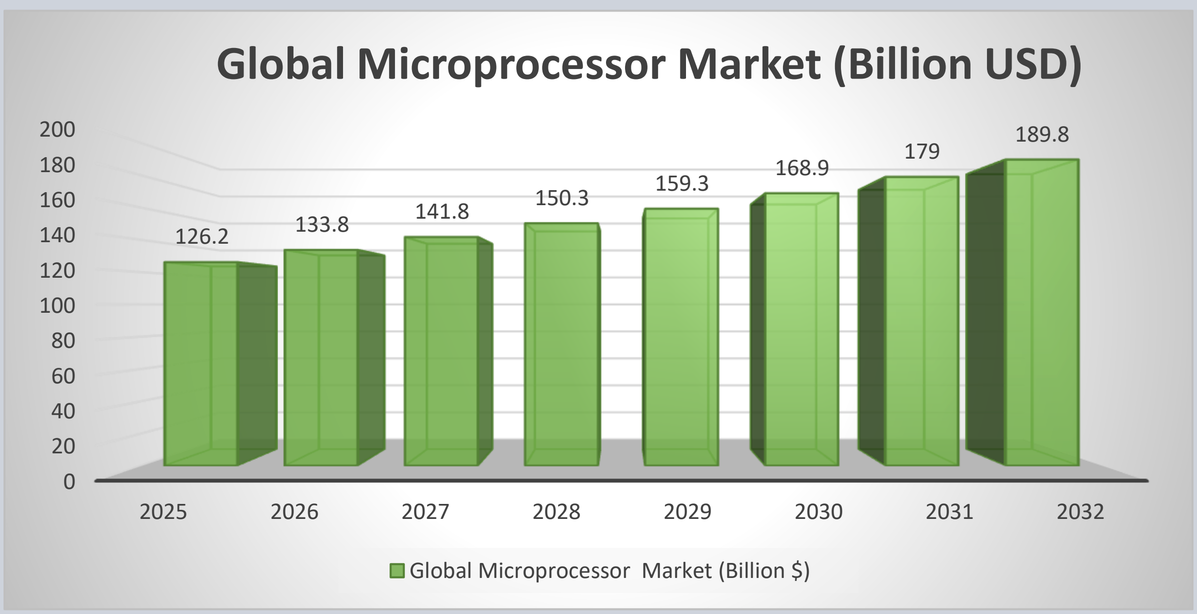
• Microprocessor (Processor ICs) Market Overview

The global microprocessor market is expanding rapidly, fueled by growing demand for high-performance computing, IoT, 5G, AI, and automotive applications such as infotainment and ADAS. **Within this market, adders are indispensable components of microprocessor architecture, driving arithmetic operations that determine processing speed and efficiency.** They enable essential tasks like addition, subtraction, and logical processing, making them fundamental to the overall operation and reliability of microprocessors.

The global Microprocessor (Processor ICs) market was valued at USD 126.25 Billion by 2025. Looking further ahead, the market is expected to grow significantly, reaching an estimated USD 189.83 Billion by 2032. This growth reflects a robust compound annual growth rate (CAGR) of 6% during the period from 2025 to 2032.

Rising demand for high-performance, energy-efficient solutions is accelerating the adoption of customized processors. Industries such as automotive, healthcare, consumer electronics, and data centers are deploying processors designed to meet specialized needs.

Advancements in adder design can significantly benefit the microprocessor market by improving processing speed, reducing power consumption, and enhancing overall efficiency. As demand grows for high-performance, low-power processors in areas like AI, IoT, and advanced consumer electronics, optimized adders can provide the necessary boost in computational capability, driving innovation and competitiveness across the market.



- <u>Microprocessor (Processor ICs) Regional Market Analysis</u>

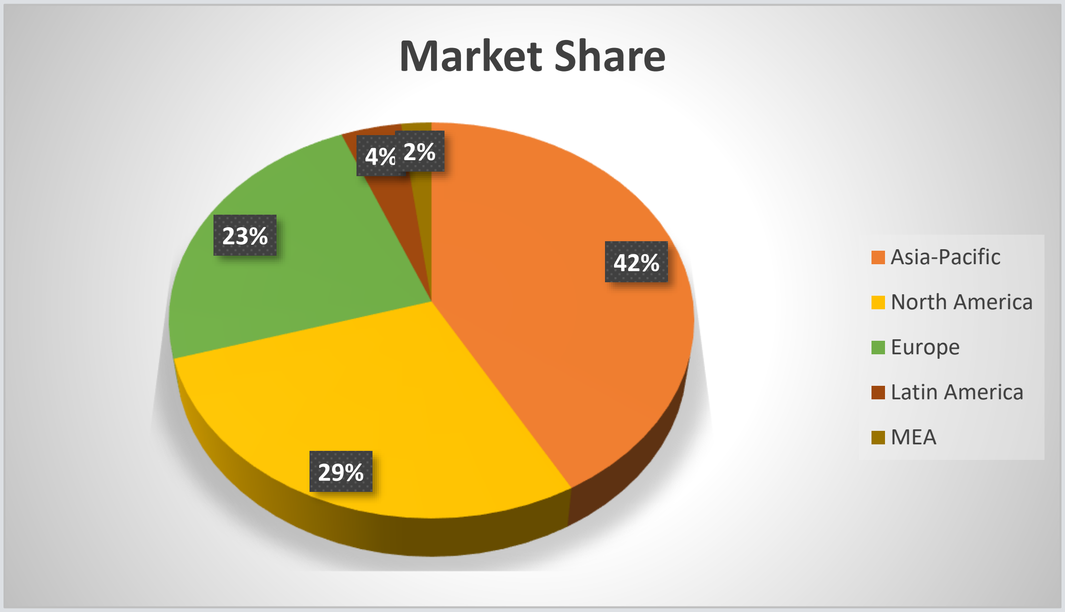
Based on geography, the microprocessor market has been divided across Asia Pacific, North America, Europe, Latin America and the Middle East & Africa.

Asia Pacific dominates the global market with a leading share of 43%, followed by North America, which holds 28% of the market. Europe captures 23%, positioning it as the third-largest regional player. The remaining market share is distributed across the Latin America with 4% market and Middle East & Africa with 2% market. Together, these regions shape the overall dynamics of the global market.

China dominates the Asia Pacific market with its robust semiconductor manufacturing ecosystem, backed by extensive foundries, assembly facilities, and well-established supply chain networks.

North-America holds a strong presence in the market due to strong presence of leading players, including intel, AMD, Nvidia and Qualcomm. Strong investment in R&D, along with the rapid uptake of advanced technologies like AI and edge computing, is fueling substantial demand across the region.

Europe market is driven by strong automotive sector, where modern microprocessors are essential for powering electric mobility and enabling autonomous driving technologies. The Middle East & Africa and South America are projected to see slower market growth, constrained by economic uncertainties and relatively limited progress in industrial and technological infrastructure.



• Application Specific Integrated Circuit (ASICs) Market Overview

The global ASIC chip market is witnessing strong momentum as demand grows for customized integrated circuits that deliver higher performance with improved energy efficiency. Application-Specific Integrated Circuits (ASICs) are increasingly being developed to serve targeted applications, including AI accelerators, automotive electronics, and mobile devices. Their ability to optimize processing for specific tasks is driving widespread adoption across multiple industries.

The global Application Specific Integrated Circuit (ASICs) market was valued at USD 22.35 Billion by 2025. Looking further ahead, the market is expected to grow significantly, reaching an estimated USD 37.08 Billion by 2032. This growth reflects a robust compound annual growth rate (CAGR) of 7.38% during the period from 2025 to 2032.

The growing adoption of smartphones, tablets, and wearable devices is fueling the expansion of the ASIC market. Since ASICs are developed for domains such as AI acceleration, networking, and automotive systems, **improvements in adders directly translate into better computational throughput, reduced energy costs, and enhanced efficiency. This makes innovation in adder technology a key enabler for sustaining the growth and competitiveness of the ASIC market.**

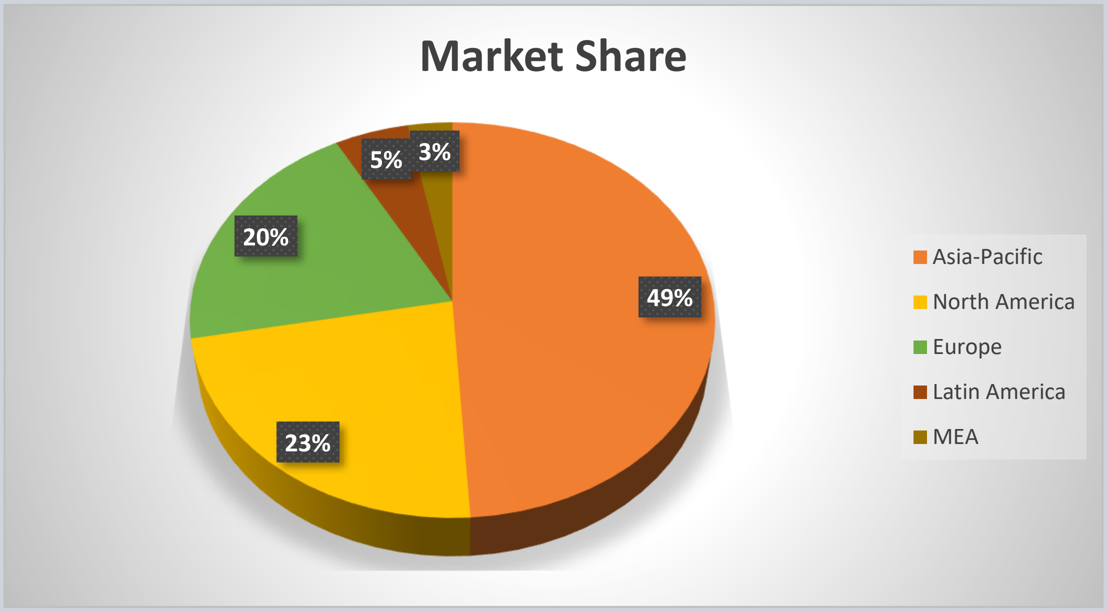
- **Application Specific Integrated Circuit (ASICs) Regional Market Analysis**

The global Appication Specific Integrated Circuit (ASICs) market is segmented into North America, Europe, Asia Pacific, Latin America and Middle East & Africa, each showing unique growth drivers.

Asia Pacific dominates the global market with a leading share of 49%, followed by North America, which holds 23% of the market. Europe captures 20%, positioning it as the third-largest regional player. The remaining market share is distributed across the Latin America with 5% market and Middle East & Africa with 3% market. Together, these regions shape the overall dynamics of the global market.

The rising need for energy-efficient devices, coupled with the growing use of smartphones in the region, is accelerating market growth. Furthremore, the emergence of Electric Vehicles (EVs), Advanced Driver Assistance Systems (ADAS), and autonomous driving technologies has significantly reshaped the automotive industry, creating strong momentum for the growth of the ASIC market.

Some notable players in the Application Specific Integrated Circuit (ASICs) market Advance Micro Devices Inc, Infineon Technologies, Intel corporation, Nvidia Corporation, Samsung Electronics Co Ltd, Texas Instruments, Analog Devices and ST Microelectronics.

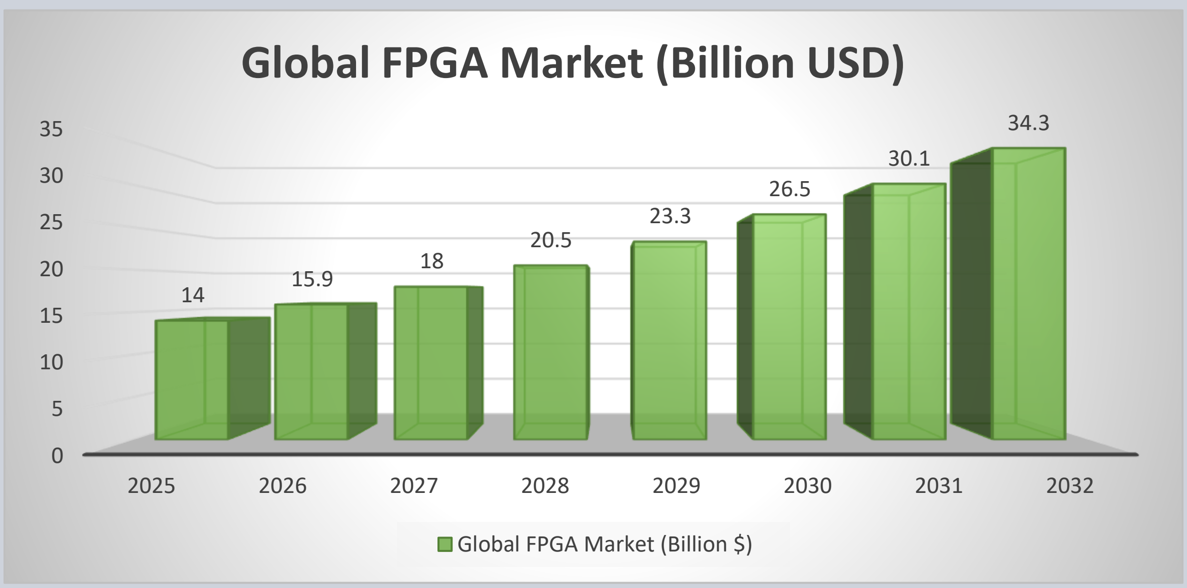


• FPGAs & Programmable Logic Devices Market Overview

Field-Programmable Gate Arrays (FPGAs) are versatile semiconductor devices that can be reprogrammed to perform a wide range of tasks. **Within their architecture, adders form a fundamental component, enabling the arithmetic operations** required in applications such as digital signal processing, AI acceleration, and cryptography. Implemented through dedicated carry chains and logic blocks, **adders directly influence the speed, efficiency, and overall computational capability of FPGAs.**

The global Field-Programmable Gate Arrays (FPGAs) market was valued at USD 14 Billion by 2025. Looking further ahead, the market is expected to grow significantly, reaching an estimated USD 34.3 Billion by 2032. This growth reflects a robust compound annual growth rate (CAGR) of 13.66 % during the period from 2025 to 2032.

The FPGA market is witnessing strong growth, fueled by the rising demand for reconfigurable solutions that deliver both high performance and energy efficiency. **Adders play a critical role in this progress, as advanced adder architectures significantly boost the computational capabilities of FPGAs.** Their importance extends beyond functionality, positioning them as a key driver of market expansion across industries such as telecommunications, automotive, and aerospace.



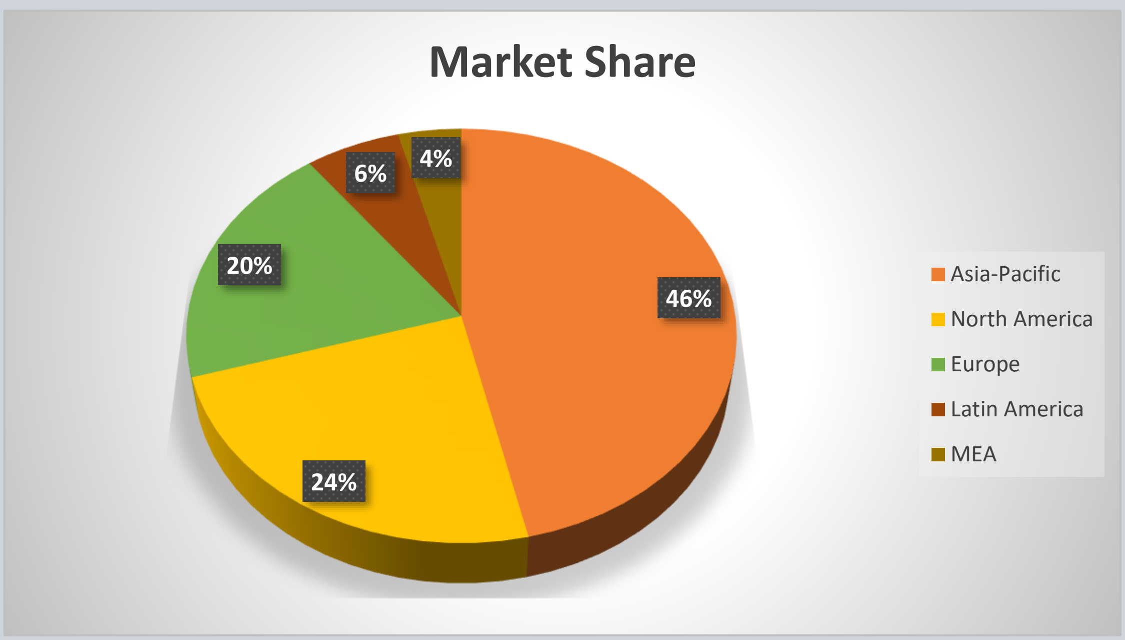
- <u>FPGAs & Programmable Logic Devices Regional Market Analysis</u>

The global Field-Programmable Gate Arrays (FPGAs) market is segmented into North America, Europe, Asia Pacific, Latin America and Middle East & Africa, each showing unique growth drivers.

Asia Pacific dominates the global market with a leading share of 47.5%, followed by North America, which holds 23.4% of the market. Europe captures 19.1%, positioning it as the third-largest regional player. The remaining market share is distributed across the Latin America with 6% market and Middle East & Africa with 4% market. Together, these regions shape the overall dynamics of the global market.

The FPGA market shows diverse regional growth patterns worldwide. The Asia Pacific region is emerging as the largest contributor to the FPGA market, driven by rapid digital transformation, smart city initiatives, and widespread automation across industries. North America follows closely, supported by advanced infrastructure, high R&D investment, and strong demand in defense and aerospace. Europe maintains steady growth, led by Germany's focus on automotive technologies and the region's push for sustainable, energy-efficient electronics.

Latin America is gradually expanding, with digital transformation and adoption of IoT and AI in industries like agriculture and manufacturing driving FPGA demand. Meanwhile, the Middle East & Africa are in the early stages of growth, fueled by investments in 5G, industrial automation, and smart infrastructure.



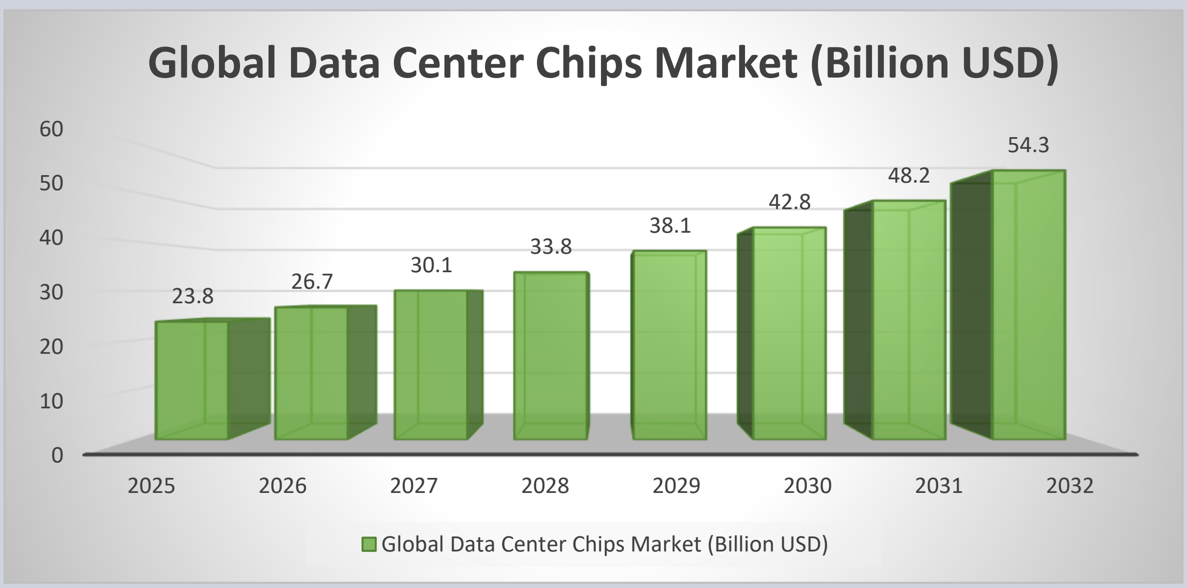
- ## Data Center Chips Market Overview

A data center chip is a specialized semiconductor designed to power the high computational and processing needs of servers. These chips are designed to handle the heavy computational and processing demands of modern servers. **Within these architectures, adders form a fundamental part of arithmetic and logic operations, ensuring fast and efficient execution of critical tasks.** Their role in accelerating calculations makes them indispensable to meeting the performance and efficiency needs of large-scale data processing and cloud-based applications.

The global Data Center Chips market was valued at USD 23.8Billion by 2025. Looking further ahead, the market is expected to grow significantly, reaching an estimated USD 54.3 Billion by 2032. This growth reflects a robust compound annual growth rate (CAGR) of 12.5 % during the period from 2025 to 2032.

Enhancements in adder circuit design play a vital role in advancing data center chips by delivering faster computation with lower power consumption. As efficiency and scalability become top priorities in data centers.

At the same time, the surge in AI, ML, and IoT applications is driving unprecedented demand for high-performance chips. These technologies generate vast datasets and require specialized hardware capable of handling complex algorithms, real-time analytics, and large-scale storage, further fueling the growth of the data center chip market.



- **Data Center Chips Regional Market Analysis**

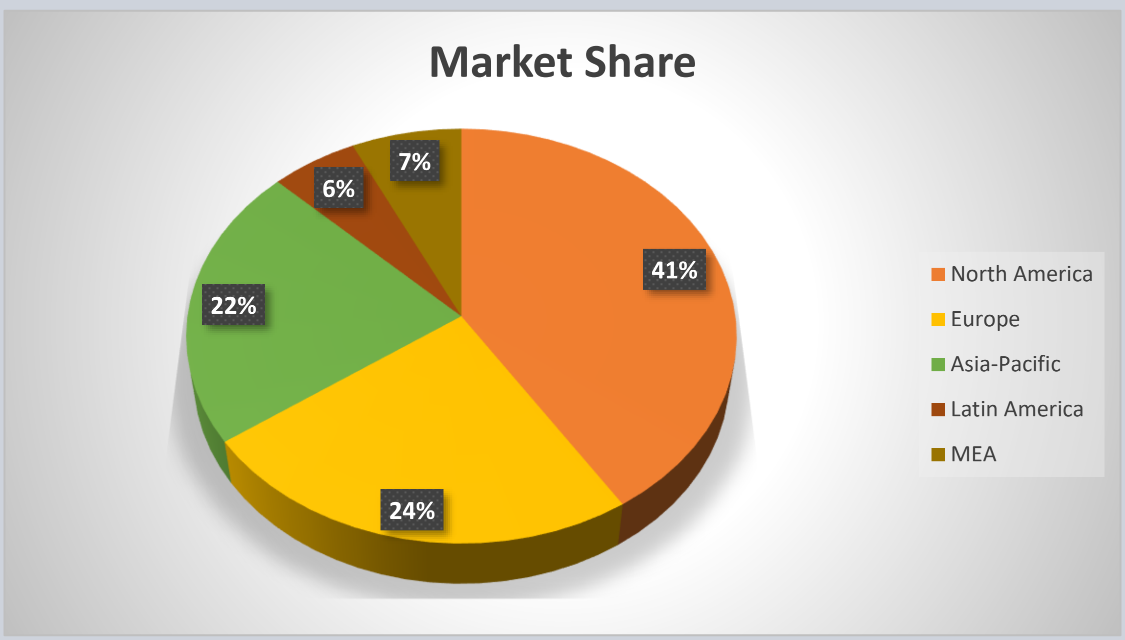
The global Data Center Chips market is segmented into North America, Europe, Asia Pacific, Latin America and Middle East & Africa, each showing unique growth drivers.

North America dominates the global market with a leading share of 40.9%, followed by Europe, which holds 24.3% of the market. Asia-Pacific captures 22.1%, positioning it as the third-largest regional player. The remaining market share is distributed across the Latin America with 5.6% market and Middle East & Africa with 7.1% market. Together, these regions shape the overall dynamics of the global market.

North America market is supported by its strong infrastructure, heavy R&D investments, and high demand from major tech firms and financial institutions. Its early adoption of advanced technologies further strengthens its position.

Europe maintains a strong position in the data center chip market, supported by its advanced IT infrastructure, strict data privacy regulations, and sustained investments in modern facilities while Asia Pacific is set to grow at the fastest pace, driven by rapid digitalization, widespread cloud adoption, and substantial investments from governments.

The Middle East & Africa are set for strong growth with rising cloud adoption and government digital initiatives, while South America grows moderately, limited by economic and adoption challenges.



APPLICATION AREAS

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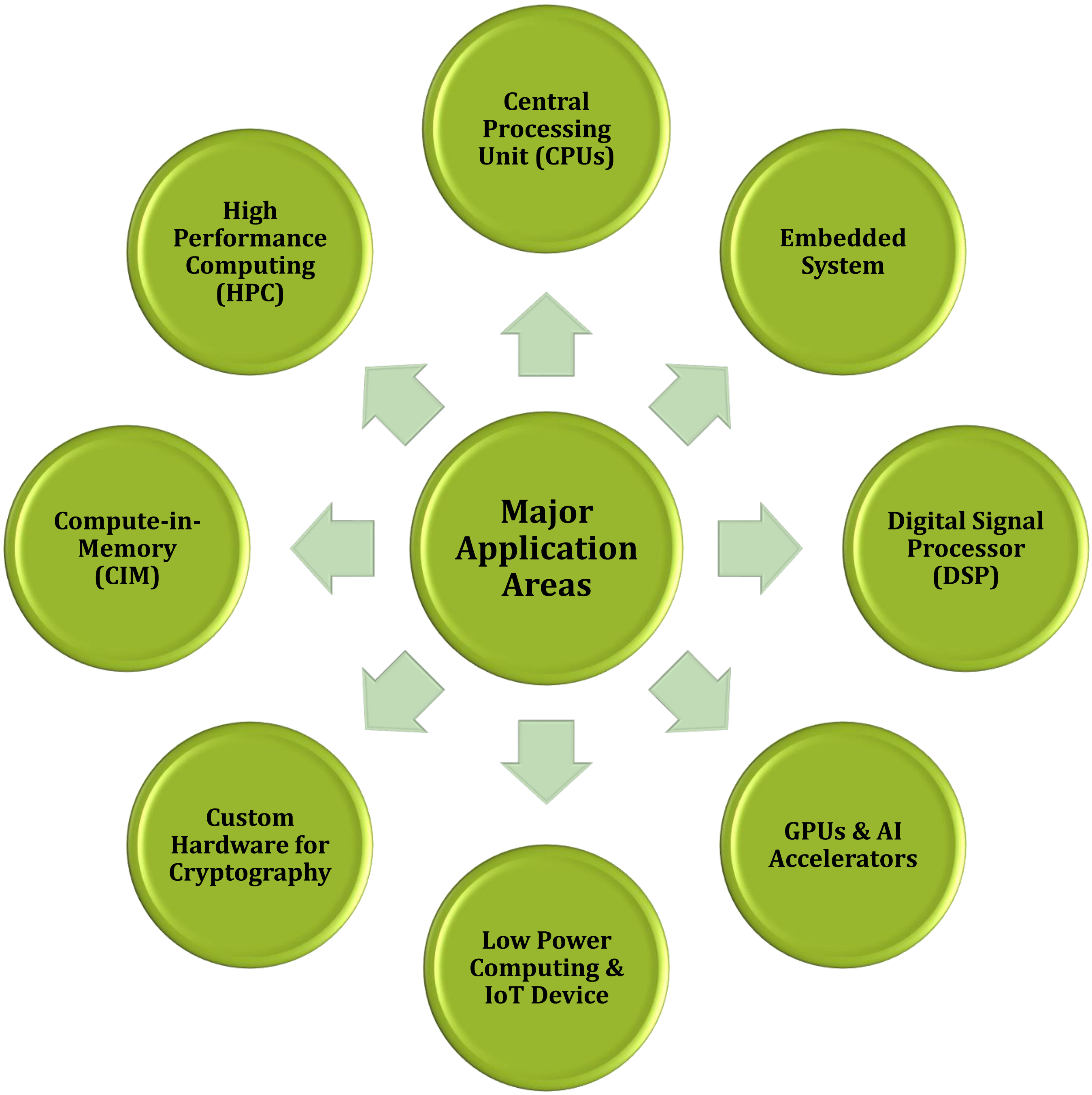
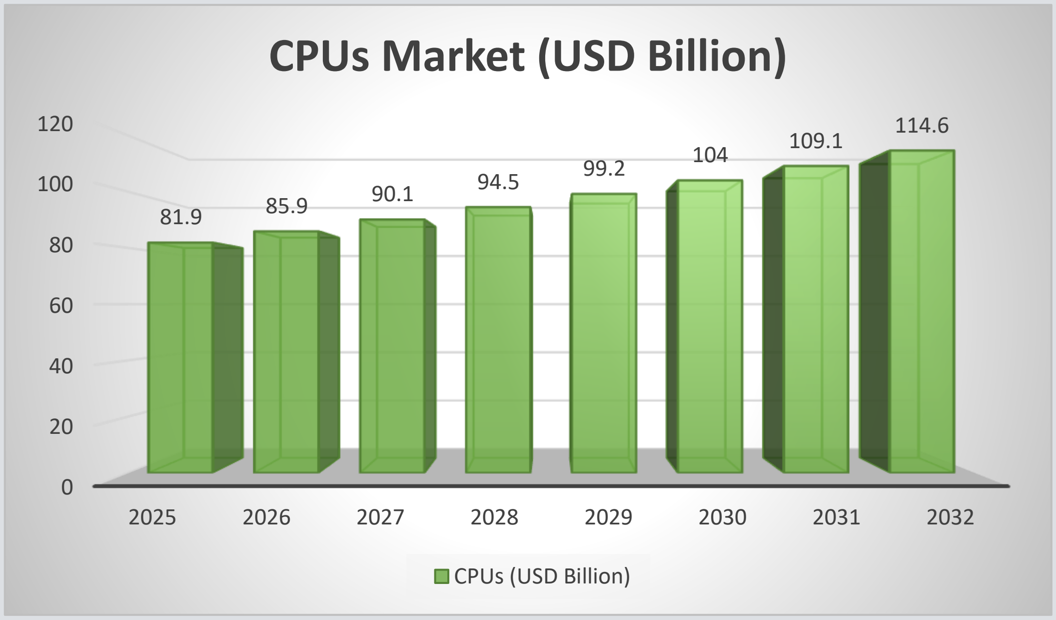

Major Application Areas
Central Processing Unit (CPUs)
Embedded System
Digital Signal Processor (DSP)
GPUs & AI Accelerators
Low Power Computing & IoT Device
Custom Hardware for Cryptography
Compute-in-Memory (CIM)
High Performance Computing (HPC)

A. Central Processing Unit (CPUs) Market



The growth of the Central Processing Unit (CPU) market is driven by increasing demand for high-performance computing, advancements in technology, and the proliferation of IoT devices. With the constant evolution of artificial intelligence and machine learning, the need for more powerful and efficient CPUs has become paramount, further fueling market growth. **In the Central Processing Unit (CPU), the adder is a crucial component responsible primarily for performing addition operations.** The adder is an integral part of the Arithmetic Logic Unit (ALU)**,** where it enables the CPU to carry out essential calculations such as addition, subtraction (using techniques like two's complement), and value comparison.

The global CPU market size was valued at USD 81.9 billion in 2025 and is projected to reach USD 114.6 billion by 2032, growing at a compound annual growth rate (CAGR) of 4.9% during the forecast period.

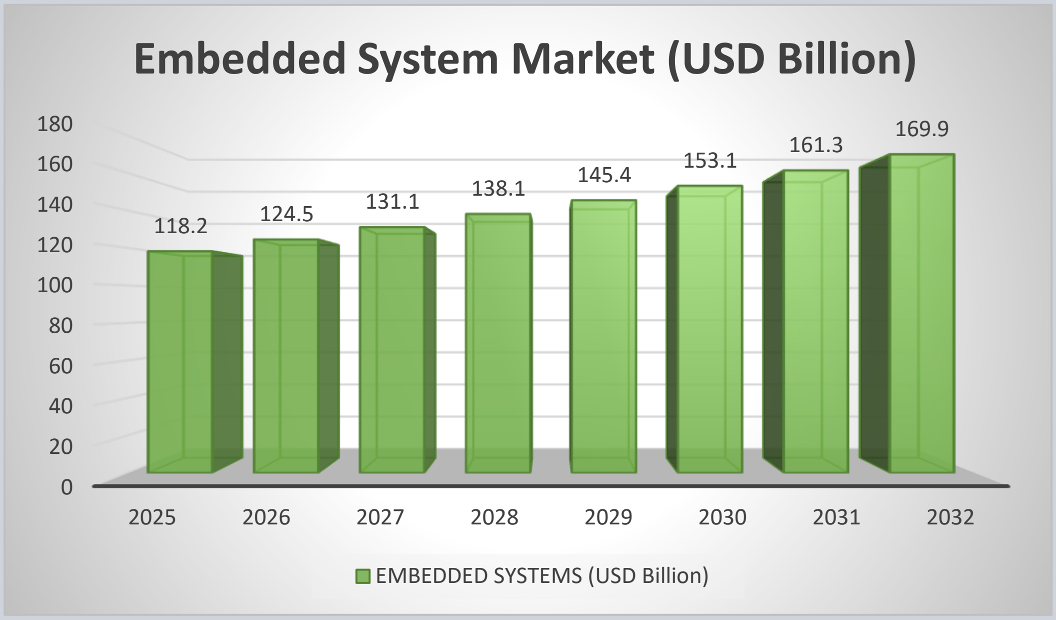
This market is driven by the increasing demand for advanced computing technologies in industries including consumer electronics, automotive, healthcare, telecommunications, and industrial automation. Key players in the market include Intel, AMD, and Qualcomm, among others, along with emerging competitors. The market is characterized by rapid technological advancements, including smaller transistor nodes, improved energy efficiency, and integration of artificial intelligence capabilities.

➢ Benefits In CPUs Using Simple Linear Fast Adder

Current Central Processing Unit (CPUs) typically use complex adders like carry-lookahead or carry-select adders that parallelize carry prediction to speed computations. These designs focus on minimizing carry propagation through parallelism but involve more complex circuitry. The Simple and Linear Fast Adder improves addition speed by computing addition in terms of a novel addition algorithm. This algorithm is implemented in a sequential logic circuit that works like a finite state machine that reaches a stable state in logarithmic time. The topology is simple and linear, reducing power use, and chip size — while still delivering high performance, especially in floating-point units. It's a more efficient and faster option for key addition tasks in central processing units.

- ✓ It's simple design means the circuit is less complex, is easier to design and manufacture, and uses less power than traditional adders.
- ✓ It speeds up important parts of the central processing units by reducing delays during addition, a common and time-sensitive task in math and floating-point operations.
- ✓ By making addition and rounding faster, it helps the processor run more efficiently and improves overall performance, especially in tasks like floating-point multiply-add operations.

B. Embedded System Market



An embedded system is a specialized computer hardware system driven by a microprocessor, designed to fulfill a dedicated function within a more extensive system or independently. The embedded systems market is driven by the increasing demand for IoT applications, automotive electronics, and industrial automation. Also, advancements in technology, especially in wireless communication, will boost the adoption of such systems.

The* embedded systems *market was valued at USD 118.2 billion in 2025 and is expected to grow to USD 169.9 billion by 2032, registering a compound annual growth rate (CAGR) of 5.31% over the forecast period.

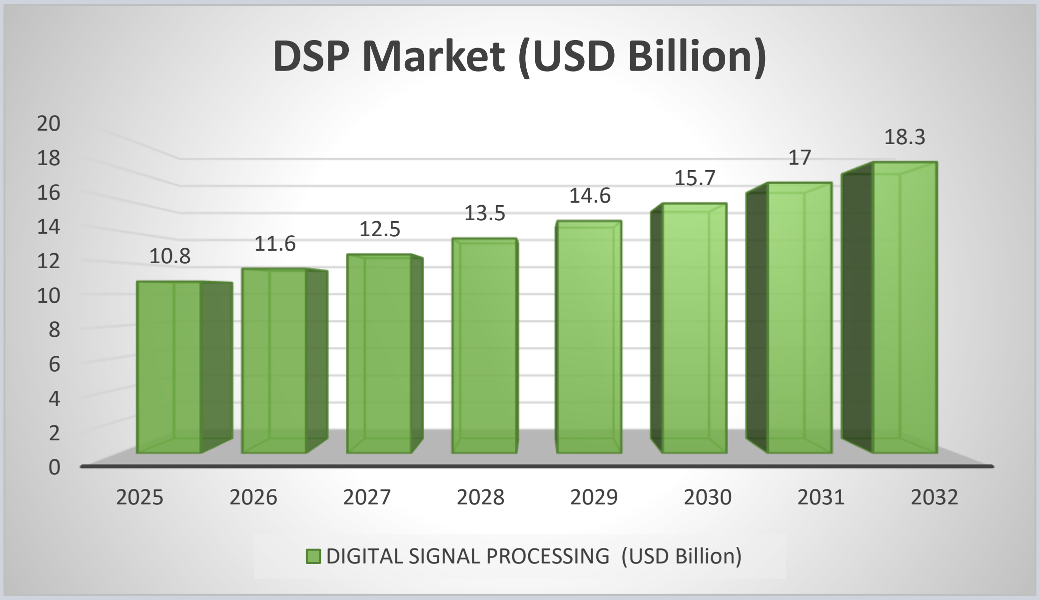
The embedded systems market is expanding rapidly, fueled by the rising demand for smart and connected solutions in sectors such as automotive, healthcare, and industrial automation. With AI and machine learning increasingly being integrated into these systems, the need for efficient computation is higher than ever. **Adders play a crucial role in this architecture, with designers selecting specialized types based on application requirements**—Ripple Carry Adders for ultra-low-power devices, Carry Look-Ahead Adders for high-speed automotive and industrial control, Carry-Save Adders for parallel data processing, and Carry Select Adders for achieving a balance between speed and hardware efficiency. This adaptability makes optimized adder design a foundation for advancing embedded system performance across diverse use cases.

➢ Benefits In Embedded Systems Using Simple Linear Fast Adder

Current Technology in embedded systems use complex adders to speed up addition, but these take more space, use more power, and are harder to design. Our new adder uses a simple, step-by-step method to iterate two bit columns until the addition is calculated and saved in one of these columns. It's smaller, uses less power, and is easier to build. This makes it a fast, efficient, and reliable solution for embedded systems where saving space and power is important.

- ✓ The adder uses a simple design, which makes the circuit less complicated. This means it takes up less space on the chip and uses less power important for small, low-power embedded systems.
- ✓ The simpler design makes the hardware more reliable and easier to add to microcontrollers, DSPs, and other embedded processors. This helps speed up development and can reduce costs.
- ✓ By making addition faster and using less power, it helps embedded systems work quickly and run longer on limited battery power.
- ✓ It handles rounding in floating-point calculations well, which helps improve performance in tasks like signal processing, control, and communication that are common in embedded devices.

C. Digital Signal Processing (DSP) Market



Digital signal processors (DSP) are specialist microprocessors that, unlike general-purpose microprocessors, have an architecture optimized for digital signal processing operations using voice, video, audio, temperature, and location signals. **In Digital Signal Processors (DSPs), key components such as the Arithmetic Logic Unit (ALU), multipliers, registers, and memory work together for high-speed computations, with adders serving as a critical part of the DSP architecture to enable efficient arithmetic operations essential for signal processing tasks.**

The digital signal processing market is experiencing significant growth in all regions, driven by technological advancements and the growing demand for high-performance computing.

The Global Digital Signal Processor Market Size was Valued at USD 10.8 Billion in 2025. The Market Size is anticipated to Exceed USD 18.3 Billion by 2032, growing at a CAGR of 7.89% from 2025 to 2032.

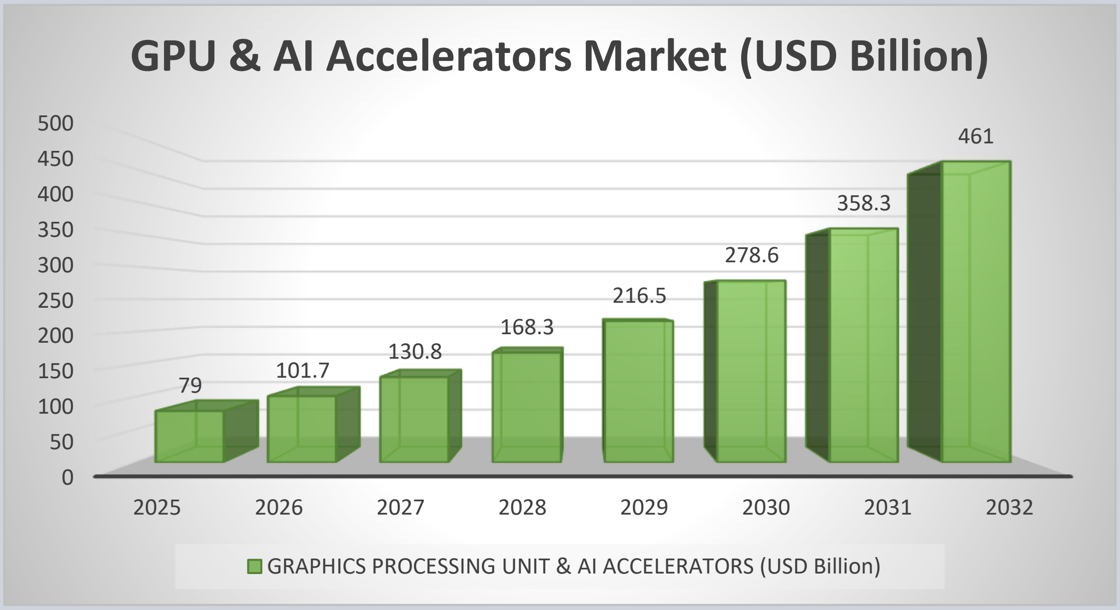
Furthermore, the digital signal processor market is being fuelled by a number of reasons, including the rising need for advanced signal processing in a variety of industries, the expansion of Internet of Things (IoT) technology, and the rising demand for high-quality audio and video processing. The market is also being driven by increased DSP adoption in emerging economies, as well as the development of new and innovative DSP technologies.

➢ Benefits In DSP Market Using Simple Linear Fast Adder

Most Digital Signal Processing (DSP) units today use complex adders like carry-lookahead or carry-select adders. These adders speed up addition by working on carry bits in parallel and doing some steps ahead of time. They generate carry signals in stages using layered or tree-like logic, which helps add large numbers quickly. But, because of this complexity, they take up more chip space, use more power, and are harder to design. Our FAU core is linear and has a simple to integrate and manufacture layout. This makes it a fast and efficient choice for DSP applications.

- ✓ It makes addition faster, which helps speed up processing in DSP systems.
- ✓ It has a simple design with fewer parts, so it takes up less space on the chip and uses less power.
- ✓ The compact design helps save space and energy—great for small and low-power DSP devices.
- ✓ Because it uses less power and chip space, it helps DSP systems run better, especially in tasks that need fast and reliable results.
- ✓ It doesn't wait for lower bits to finish before moving to higher ones, so the whole addition happens faster.

D. Graphics Processing Unit & Ai Accelerators Market



Graphics Processing Units (GPUs) were originally designed to accelerate video rendering and image processing but have rapidly expanded into broader applications such as gaming, parallel computing, and AI. Their massively parallel structure makes them highly effective for handling complex algorithms and large datasets in modern computing environments.

Adders are integral to the architecture of GPUs and AI accelerators, enabling the fast arithmetic operations required for graphics rendering, large-scale data handling, and AI model execution. Optimizing adder circuits not only improves computational throughput but also enhances energy efficiency, positioning them as a key enabler in the future growth of GPU and AI accelerator markets.

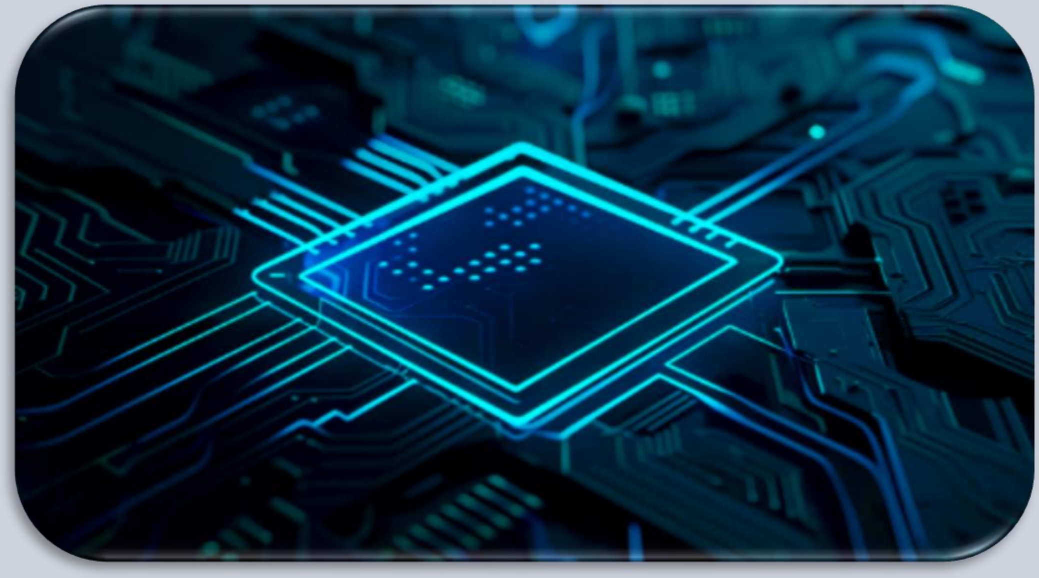
The global graphic processing unit (GPU) market size was valued at USD 79 billion in 2025 and is projected to grow USD 461 billion by 2032, exhibiting a CAGR of 28.6% during the forecast period.

This rapid expansion is fueled by increasing demand for high-performance computing, AI workloads, and data-intensive applications across industries. North America, which accounted for the largest share at 34.99% in 2023, is expected to maintain a strong position due to its advanced technological infrastructure and leadership in AI innovation. As AI accelerators become essential for powering next-generation applications, the combined GPU and AI accelerator market will continue to be a key driver of digital transformation worldwide.

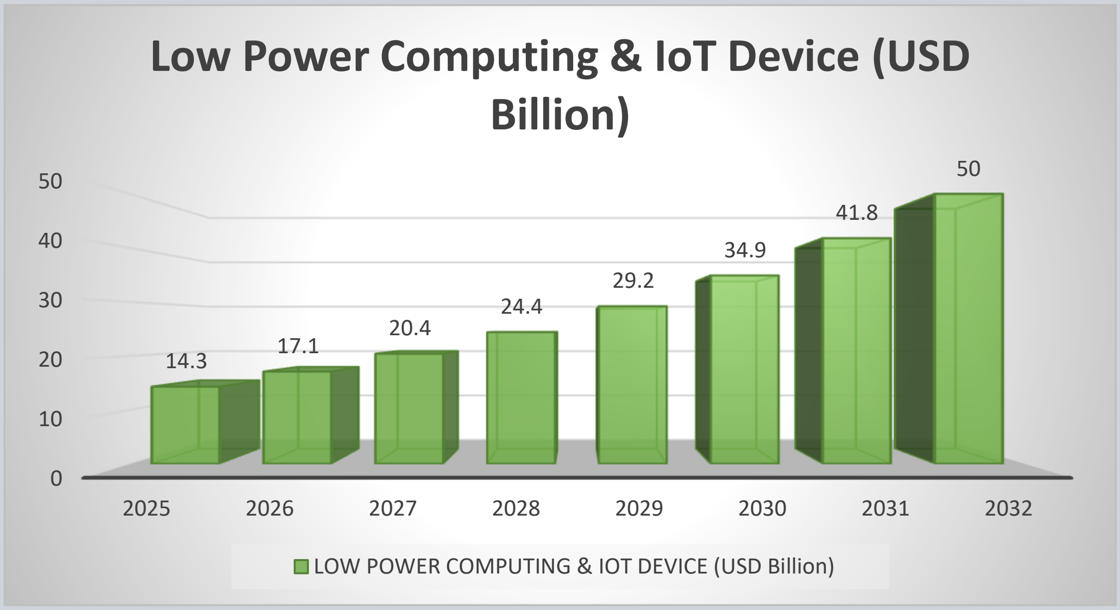
➢ Benefits In GPUs & AI Accelerator Using Simple Linear Fast Adder

Most GPUs and AI chips today use complex adders like carry-lookahead and carry-select to make addition faster. But these designs are large, use more power, and are harder to build and connect with other parts. Our design also allows for a regular rectangular grid array in rows and columns that executes fast multiplication, and addition of multiple inputs. Memory and Arithmetic-Logic transistors can be placed next to each other in one-to-one correspondence, eliminating migration time and energy altogether. This design is scalable to achieve fast and efficient In-Situ Matrix Multiplication with optimized area. This adder is smaller, uses less power, and is easier to use in designs. It's a good fit for AI and GPU systems that need to be fast, efficient, and compact.

- ✓ The simple linear fast adder enables faster arithmetic computations essential in GPU and AI accelerator cores for matrix operations and parallel processing.
- ✓ Faster adder circuits increase the processing throughput of AI accelerators, allowing quicker execution of deep learning inference and training tasks
- ✓ In GPUs, the fast adder decreases latency in pixel shading and compute-heavy rendering pipelines through rapid arithmetic operations.
- ✓ The simplified linear logic reduces switching activity and power consumption compared to conventional adders, benefiting energy-constrained AI accelerators and mobile GPUs.
- ✓ The design allows for a compact adder implementation, saving silicon area in GPUs and AI chips, which can be used to enhance other processing units or add more cores.
- ✓ The linear adder can be generalized to a rectangular memory grid that can execute In-Situ addition of multiple inputs, and therefore multiplication of two inputs.
- ✓ The rectangular design is especially well suited for scalability to achieve fast and energy efficient matrix multiplication in optimized area.



E. Low-Power Computing & IoT Devices Market



The global Low Power IoT market size was valued at approximately $14.3 billion in 2025 and is projected to reach around $50 billion by 2032, growing at an impressive CAGR of 20% during the forecast period.

This rapid expansion of this market is primarily driven by the increasing demand for energy-efficient solutions in various applications, from smart homes to industrial IoT systems. As the world becomes more connected and the number of IoT devices surges, the need for low power consumption technologies becomes increasingly critical, enhancing the market's growth potential.

Low-power computing systems and IoT devices increasingly rely on optimized adder designs to minimize energy consumption without compromising performance. Innovations such as the 10-transistor (10T) adder and the Static Energy Recovery Full (SERF) adder have significantly reduced transistor count and power usage, leading to enhanced computational efficiency. These advanced designs not only extend battery life but also improve processing speed, making them well-suited for compact, energy-sensitive mobile and IoT applications.

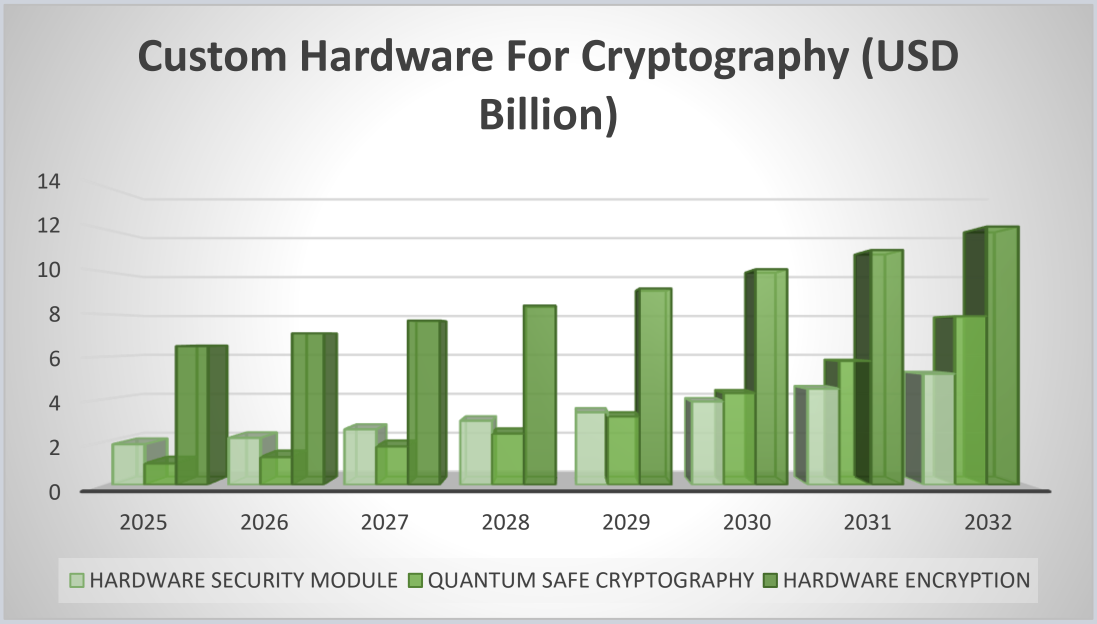
One of the major growth factors for the Low Power IoT market is the escalating adoption of smart technologies across numerous sectors. From agriculture to healthcare, IoT devices are revolutionizing operations, leading to enhanced efficiency and productivity. For instance, smart agriculture technologies enable farmers to monitor soil moisture and weather conditions in real-time, optimizing water usage and improving crop yields.

➢ Benefits In Low-Power Computing & IoT Devices Using Simple Linear Fast Adder

Current low-power computing and IoT devices use common adder designs like ripple-carry, carry-lookahead, and parallel-prefix adders. These designs try to balance speed, size, and power use. They often have different levels of circuit complexity, delays in carrying over bits, and power use that grows with the size of the numbers they handle. Our technology is different. It uses a new fast adder made of small subunits connected in series. These subunits consist of two standard logical gates (AND, XOR) and a two-bit register. This design grows in size and complexity in a simple, predictable way. It has constant gate depth, linear growth to increase bit capacity, works quickly even for bigger numbers, and can handle both whole and fractional numbers. It runs on a simple control model that makes its performance steady and energy use low, avoiding slow and power-heavy carry chains and complicated instructions.

- ✓ The adder saves energy and helps devices last longer on batteries.
- ✓ The compact design uses fewer parts, saving space on small IoT chips and edge devices.
- ✓ Built from small identical blocks connected in series. The design grows in a simple, straight line as numbers get bigger, making it easy to expand and build.
- ✓ It can do extra tasks like shifting bits and handling signed numbers without needing extra hardware, keeping the computing unit simple.
- ✓ It follows a simple control model that makes it reliable, predictable, and easy to fit into custom device designs.

F. Custom Hardware for Cryptography Market



Custom hardware for cryptography is increasingly vital as data protection demands grow across financial, defense, and enterprise applications. **At the heart of these architectures, adders enable the rapid execution of arithmetic operations essential for encryption, decryption, and key generation, directly influencing performance and security.** The market spans multiple divisions, including hardware encryption for secure data transfer, hardware security modules (HSMs) for safeguarding cryptographic keys, and emerging quantum-safe cryptography designed to withstand post-quantum threats.

i. HARDWARE SECURITY MODULES MARKET SIZE:

The global hardware security module market was valued at $1.9 billion in 2025, and is projected to reach $5.2 billion by 2032, growing at an impressive CAGR of 14.7% during the forecast period.

ii. QUANTUM-SAFE CRYPTOGRAPHY MARKET SIZE:

The global Quantum-safe cryptography market size was valued at USD 1 billion in 2025. The market is projected to grow from USD 7.9 billion by 2032, exhibiting a CAGR of 34.7% during the forecast period 2025-2032.

iii. HARDWARE ENCRYPTION MARKET SIZE:

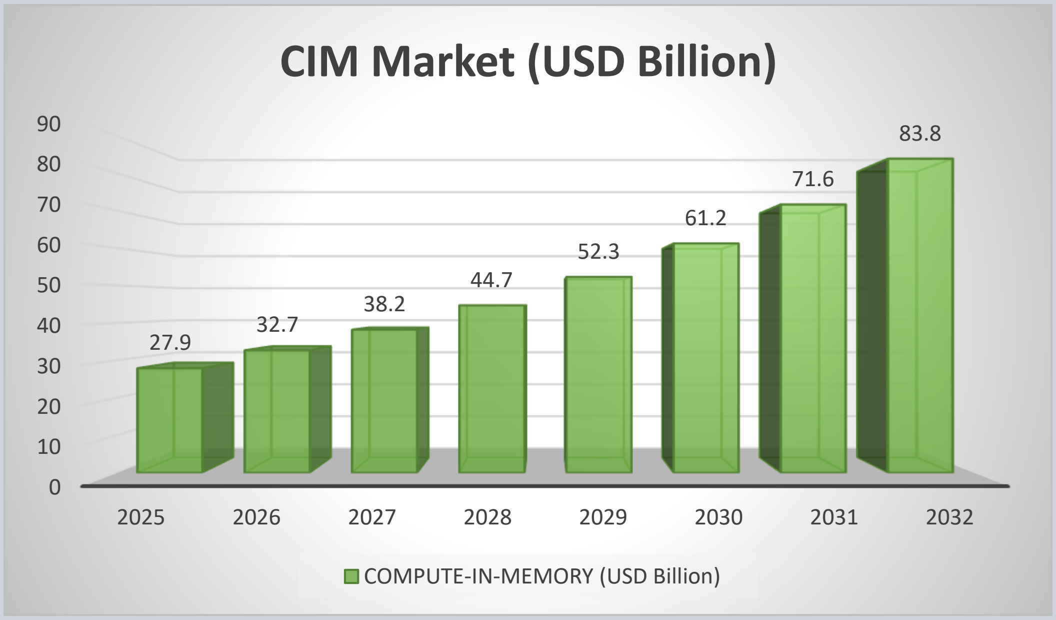
The global hardware encryption market size was valued at USD 6 million in 2024. The market is projected to grow from USD 6.5 million in 2025 to USD 12.1 million by 2032, exhibiting a CAGR of 9.26% during the forecast period

➢ Benefits In Custom Hardware for Cryptography Using Simple Linear Fast Adder

Current cryptographic hardware often uses adders like ripple-carry or carry-lookahead, which slow down and use more power as numbers get bigger. This creates delays in custom hardware, encryption systems, and security modules, especially with growing demands from quantum-safe algorithms. Our technology uses a simple, linear design built from small logic blocks and registers. It runs fast, stays energy-efficient, and uses consistent power even with large numbers. In custom hardware, it reduces delay and saves chip space. In hardware encryption, it boosts speed and lowers energy use. In Hardware Security Module, it improves performance without adding complexity. It also supports quantum-safe cryptography by handling large numbers efficiently and with predictable timing helpful for security against side-channel attacks.

- ✓ The simple linear fast adder reduces carry propagation delay by using a direct, linear computation approach, enabling faster and more predictable cryptographic operations.
- ✓ This adder's design is scalable and grows uniformly with operand size, simplifying hardware implementation across different key lengths.
- ✓ It offers low and consistent power consumption, making it ideal for energy-efficient custom cryptographic chips.
- ✓ Constant timing behavior helps protect against timing-based side-channel attacks, enhancing hardware security.
- ✓ The adder supports large-bit arithmetic efficiently, making it well-suited for post-quantum cryptography algorithms requiring heavy modular operations.

G. Compute-In-Memory (CIM) Market



Compute-in-Memory (CIM) architectures consist of several key components that work together to perform computations directly within memory. These components include memory cells, control logic, sense amplifiers, and adders. **Adders are essential in CIM because they handle all arithmetic operations required for processing data within the memory itself.**

The in-memory computing market is growing rapidly, driven by the increasing demand for faster processing capabilities and instant data analysis in fields such as finance, healthcare, and telecommunications. This market encompasses a range of products including in-memory data grids, in-memory databases, and in-memory analytics, all designed to provide high-speed, scalable, and efficient data processing solutions.

The Global In-Memory Computing Market size is expected to be worth around USD 83.8 Billion by 2032, from USD 27.9 Billion in 2025, growing at a CAGR of 17% during the forecast period from 2025 to 2032. In 2023, North America dominated the in-memory computing market, capturing over 37% of the market share, with revenues totaling USD 7.5 billion.

In 2023, the Solutions segment led the in-memory computing market with over 68% share, driven by technologies such as in-memory databases, data grids, and application platforms. Growing reliance on real-time data processing and analytics, especially in sectors demanding instant insights, continues to fuel its dominance.

➢ Benefits In Compute-In-Memory Using Simple Linear Fast Adder

Existing CIM architectures implement a variety of adders, chosen based on the specific trade-offs of the application. They can be broadly categorized by their bit-precision and their circuit style. Here's a breakdown of the most common types:

1. Low-Bit Precision / Single-Bit Adders (Dominant in Digital CIM). These are used for accumulating the single-bit partial products generated by bit-serial or bit-line computing schemes. They are simple, fast, and have a small footprint.

- Half Adders (HA) and Full Adders (FA). Trade-off: Simple and robust, but a ripple-carry chain of FAs can become a latency bottleneck for longer bit-widths.
- Parallel Prefix Adders (e.g., Kogge-Stone, Brent-Kung). Trade-off: Much faster than ripple-carry adders, but at the cost of significantly increased area, wiring complexity, and power consumption.

2. Multi-Bit / Analog-Domain Adders (Common in Analog CIM). These exploit the physical properties of circuits to perform addition on analog signals, often achieving remarkable energy efficiency.

- Charge-Sharing / Capacitive Summing is the most common technique in analog CIM. The bit-lines in a memory array have inherent capacitance. By activating multiple word-lines (representing input bits), charge from the selected cells shares on the bit-line. The resulting analog voltage is proportional to the sum of the inputs (the dot-product). Trade-off: Extremely efficient and parallel, but susceptible to noise, variations, and non-idealities. The result is an analog voltage that must be digitized by an ADC.
- Current-Summing where each memory cell (e.g., in an RRAM crossbar) acts as a programmable conductance. Applying a voltage causes a current to flow. Kirchhoff's Current Law (KCL) naturally sums these currents on the same bit-line. The total current is the analog sum of the products. Trade-off: Similar to charge-sharing: highly parallel and efficient, but analog non-idealities (line resistance, device variations) limit precision and scalability.
- Voltage-Summing / Operational Amplifier (Op-Amp) based adders using an op-amp in a summing configuration. Inputs are applied through resistors or capacitors, and the output voltage is a weighted sum. Trade-off: More accurate and controllable than passive summing, but consumes more area and power.

3. Near-Memory / In-Situ Adders. This is an emerging category that blurs the line between pure analog summing and traditional digital adders. The goal is to perform the addition within the memory array or its immediate periphery with minimal data movement, but with digital precision.

- In-Memory Majority Logic / Mux-based Adders use the memory cells themselves (e.g., 8T or 10T SRAM) not just for storage but as computational elements that can perform logic functions like majority voting, which is the core of adder carry propagation. Trade-off:

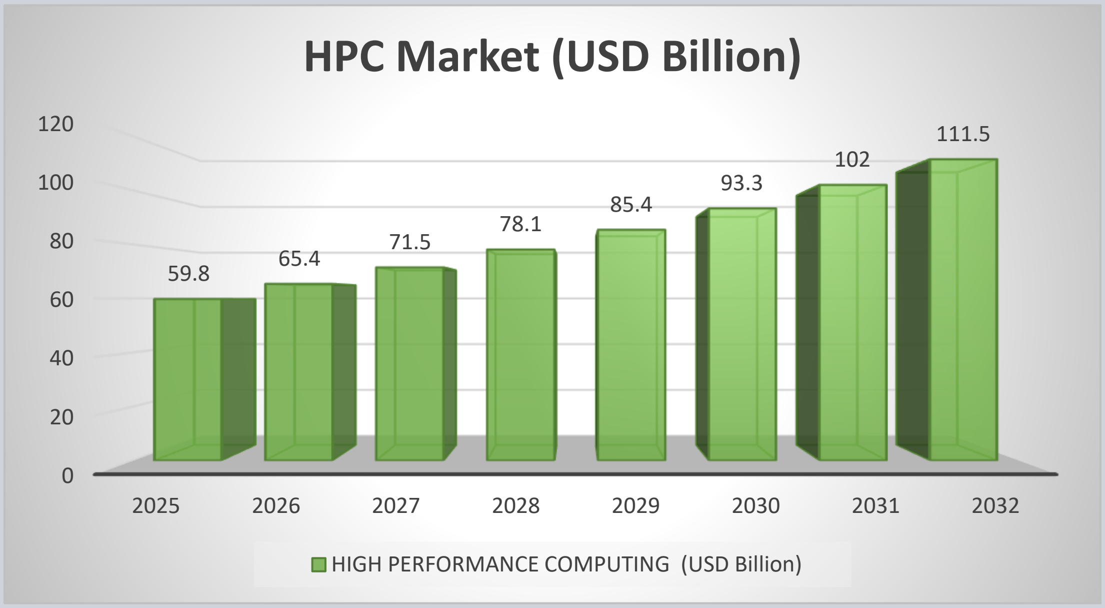
Reduces data movement to zero for that specific operation, but increases cell area and design complexity. Most practical CIM chips today use a hybrid approach: Analog summation on the bit-lines for massive parallelism, followed by simple digital adders (ripple-carry) in the periphery to accumulate the results from different segments or to handle higher precision.

- The trend is towards more sophisticated digital adders (Parallel Prefix) in the periphery as the required precision for AI models increases.

The "holy grail" of true In-Situ adders (like our proposed SLFA) that perform precise digital computation inside the array without moving data is an active and promising area of research, aiming to overcome the final bottlenecks of the Von Neumann architecture. Our architecture uses a new type of fast adder made of small identical blocks with simple logic gates and a two-bit register, connected in series. The design grows in a simple, predictable way and always uses the same amount of power, no matter how big the numbers are. It works fast even with large numbers, handles both whole and decimal numbers, and uses a simple control method. This avoids long slow chains and complex instructions, making it energy-efficient and reliable.

- ✓ The linear fast adder reduces the length of carry chains by directly computing symmetric differences and intersections, enabling faster and more predictable performance within CIM arrays.
- ✓ This technology employs a straightforward control method based on a finite state machine, enhancing reliability and simplifying integration into custom hardware.
- ✓ This technology offers a compact, power-efficient, and scalable alternative to traditional adders in Compute-in-Memory systems.
- ✓ The instruction set for this adder is constant and independent of bit-width, which helps streamline arithmetic execution in CIM environments where programmability and flexibility are often limited.

H. High Performance Computing (HPC) Market



The high-performance computing (HPC) market is expanding rapidly, fueled by the rising need for advanced simulations, big data analytics, and AI-driven applications across industries such as healthcare, finance, aerospace, and energy. HPC systems rely on massively parallel architectures to deliver exceptional speed and efficiency, enabling breakthroughs in research and innovation. **At the core of these architectures, adders serve as fundamental components for executing arithmetic operations at high speed, directly impacting system performance.** Optimized adder designs reduce latency, improve throughput, and enhance energy efficiency, making them vital for sustaining the scalability and competitiveness of the HPC market.

The global high performance computing market size accounted for USD 54.7 billion in 2024 and is predicted to increase from USD 59.8 billion in 2025 to approximately USD 111.5 billion by 2032, expanding at a CAGR of 9.3% from 2025 to 2032.

Major players in the High-Performance Computing (HPC) market, such as IBM, NVIDIA, and Intel, are driving growth through innovation, strategic collaborations, and advanced integration efforts. These companies are investing heavily in research and development to deliver greater processing power, improved scalability, and higher energy efficiency in their HPC systems. Partnerships with academic institutions and research organizations further strengthen their position, enabling the exploration of new applications and pushing the boundaries of HPC technologies to meet evolving industry demands.

➢ Benefits In High Performance Computing & IoT Devices Using Simple Linear Fast Adder

Current High-Performance Computing (HPC) systems use fast adders like carry-lookahead and prefix adders, but these become complex, power-intensive, and slower as data sizes increase due to long carry chains. This limits performance and energy efficiency in large-scale computing. Our proposed adder uses a modular design with simple logic and registers. It offers predictable scaling, constant power use, and supports both integer and floating-point operations. With simplified control and no long carry delays, it delivers superior efficiency, scalability, and reliability for next-generation HPC systems.

- ✓ This adder technology improves computational efficiency by reducing carry propagation delays, leading to faster arithmetic operations and overall system performance in high-demand HPC workloads.
- ✓ By supporting both integer and floating-point arithmetic with high speed and low power usage, the adder is well-suited for diverse HPC applications such as AI, climate modeling, and scientific simulations.
- ✓ Its modular design ensures consistent and predictable power consumption regardless of input size, enhancing energy efficiency and supporting the growing need for sustainable, power-conscious HPC infrastructure.
- ✓ The use of simple logic gates and minimalistic control logic reduces circuit complexity, resulting in lower silicon area usage and enabling more compact, cost-effective processor designs.
  Its predictable, linear performance enables easier optimization across various computing platforms, contributing to reduced development and operational costs in next-generation HPC systems.

KEY PLAYERS:

THIS PORTFOLIO CAN BE OF IMMENSE STRATAGIC USE TO BELOW MENTIONED COMPANIES

IMPLEMENTATION

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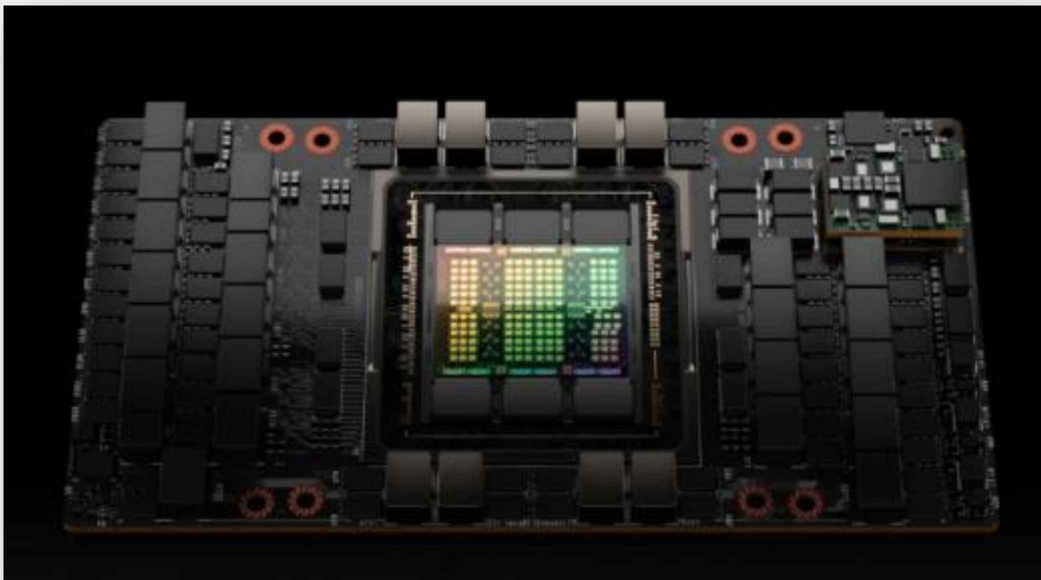
.Nvidia

The NVIDIA H100 Tensor Core GPU delivers exceptional performance, scalability, and security for every workload. H100 uses breakthrough innovations based on the NVIDIA Hopper™ architecture to deliver industry-leading conversational AI, speeding up large language models (LLMs) by 30X. H100 also includes a dedicated Transformer Engine to solve trillion-parameter language models.



NVIDIA's H100 Tensor Core GPU uses PrefixRL, an AI-driven design method, to create optimized adder circuits. By generating smaller and faster parallel prefix circuits, PrefixRL improves performance and power efficiency, enhancing the GPU's overall computational capabilities.

In PrefixRL: Optimization of Parallel Prefix Circuits using Deep Reinforcement Learning, we demonstrate that not only can AI learn to design these circuits from scratch, but AI-designed circuits are also smaller and faster than those designed by state-of-the-art electronic design automation (EDA) tools. The latest NVIDIA Hopper GPU architecture has nearly 13,000 instances of AI-designed circuits.

In PrefixRL, we focus on a popular class of arithmetic circuits called (parallel) prefix circuits. Various important circuits in the GPU such as adders, incrementors, and encoders are prefix circuits that can be defined at a higher level as prefix graphs.

i. WO2023220537A1 – Nvidia H100 Tensor Core GPU

Value-Added Enhancements of WO2023220537A1 to Nvidia H100 Tensor Core GPU

Higher Computational Throughput

By Integrating our optimized adder, the Nvidia H100 can execute arithmetic operations more efficiently, directly enhancing tensor computations. This improvement translates into faster AI training cycles and higher inference throughput, supporting the growing demand for large scale generative AI and HPC workloads.

Improved Energy Efficiency

Our adder design minimizes switching activity and power dissipation, helping the H100 operate at significantly better performance-per-watt. This improvement reduces energy costs in data centers, aligning with the industry's increasing focus on sustainability and operational efficiency.

Reduced Latency in Parallel Operations

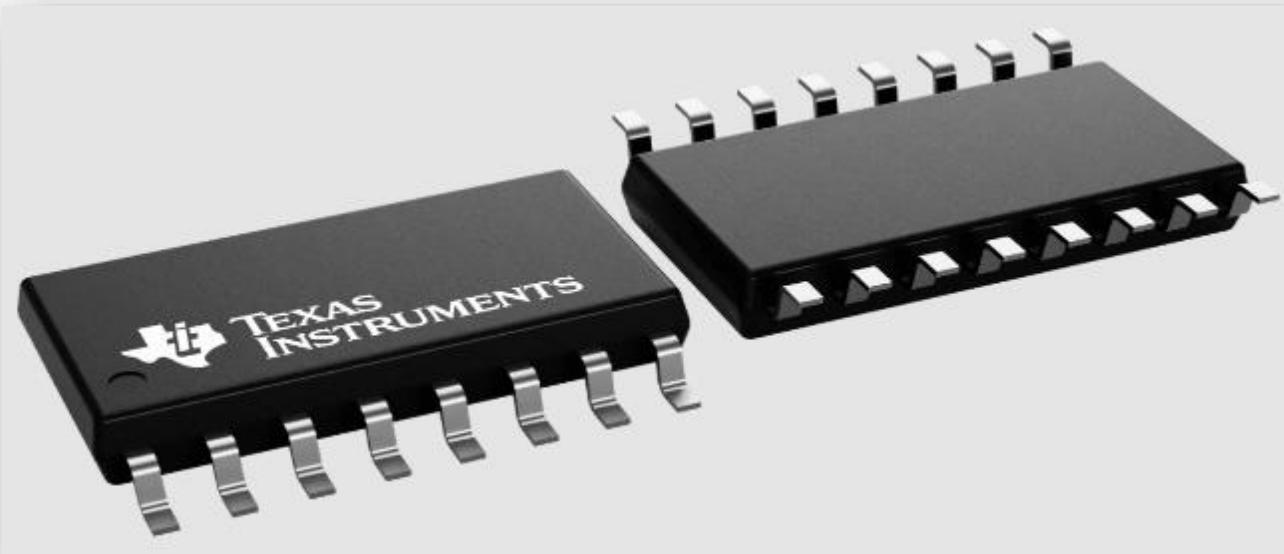
with faster carry propogation and optimized gate depth, our technology lower arithmetic latency within parallelized matrix multiplications. For the H100, this means faster execution of deep learning algorithms and more responsive performance in real-time AI applications.

Better Scalability

By lowering thermal output and power consumption, our adder enables H100 GPUs to scale more effectively in clustered environments. This benefit allows multi-GPU system to achieve greater stability, efficiency and performance.

Texas Instruments

The Texas Instruments SN74F283 is a 4-bit binary full adder with fast carry, designed to perform addition of two 4-bit binary words efficiently. It provides sum (Σ) outputs for each bit along with the carry-out (C4) from the fourth bit. The device achieves fast carry generation through full internal look-ahead logic, typically producing the carry term in about 5.7 nanoseconds, enabling high-speed arithmetic operations



This adder supports both active-high and active-low logic operands, offering flexibility in system design. It operates reliably across recommended temperature ranges from 0°C to 70°C for the SN74F283 variant, and has robust electrical characteristics suitable for various digital applications. The chip can handle supply voltages between 4.5 V and 5.5 V and delivers output currents up to 20 mA in the low state.

Packaged in multiple form factors including plastic small-outline and standard DIPs, the SN74F283 is ideal for use in digital systems requiring fast, reliable addition with integrated carry look-ahead to enhance processing speed and reduce propagation delay.

This combination of fast carry generation, versatile logic compatibility, and robust operational parameters makes the SN74F283 a trusted core component in high-performance digital circuits and computational systems

ii. WO2023220537A1 – Texas Instruments SN74F283

Value-Added Enhancements of WO2023220537A1 to Texas Instruments SN74F283

Higher Efficiency

By implementing our technology, SN74F283 achieves faster carry generation, reducing propagation delay during addition. It improves signal integrity and switching speed, allowing the adder to operate more efficiently at high speeds. These enhancements lead to quicker arithmetic operations with lower power consumption.

Scalable Design Architecture

Our technology allows the SN74F283 to be extended in a modular fashion. This enables seamless scalability from 4-bit operations to higher bit-width configurations with minimal design overhead, supporting flexible integration into larger arithmetic units or processors.

Enhanced Computational Versatility

With support for both integer operations and rational approximations of real numbers, our technology adder expands the SN74F283 arithmetic capabilities beyond basic binary addition. This makes it suitable for applications requiring mixed numeric precision or approximate computing.

Lower Power Dissipation

Our technology streamlines the logic path by minimizing redundant transitions during addition, effectively reducing dynamic power consumption. This improves the SN74F283 suitability for energy-sensitive applications delivering greater efficiency without compromising speed.

Renesas Electronics

This improved HD74HC83A full adder performs the addition of two 4-bit binary numbers. The sum (Σ) output is provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features a full internal look ahead across all four-bit generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The Renesas HD74LS83A 4-bit Binary Full Adder is a bipolar TTL device featuring fast internal look-ahead carry logic for high-speed arithmetic operations. This device is constructed with bipolar technology to ensure rapid carry generation typically around 10 nanoseconds, providing speedy overall addition performance with reduced package count.

The combination of fast carry look-ahead, TTL compatibility, and reliable construction makes the Renesas HD74LS83A a trusted choice for digital systems requiring 4-bit binary addition with high-speed and dependable performance. It is suitable for use in arithmetic units, counters, and digital logic circuits demanding quick summation and carry operations.

Renesas HD74LS83A operates within a recommended supply voltage range of 4.75 V to 5.25 V and functions reliably across an industrial temperature range from –20 °C to +75 °C. The absolute maximum ratings allow for a supply voltage up to 7 V, input voltages up to 7 V, and power dissipation up to 400 mW, ensuring durability and flexibility in varied environments.

iii. WO2023220537A1 – Renesas HD74LS83A

Value-Added Enhancements of WO2023220537A1 to Renesas HD74LS83A

Optimized Bipolar TTL Technology

The HD74LS83A utilizes bipolar TTL technology with Low Power Schottky (LS) logic, offering fast switching and reduced power consumption. The linear drive approach in our technology can complement this technology by delivering cleaner, more stable input signals helping to further minimize switching transients and enhance overall performance without compromising power efficiency.

Enhanced Speed via Fast Carry Propagation

Our technology enhances speed through optimized internal look-ahead carry logic, enabling faster carry propagation an essential factor in accelerating multi-bit binary addition when used with the HD74LS83A.

Improved Signal Integrity

Our linear drive technique enhances signal integrity by providing a cleaner, more linear input to the HD74LS83A. This reduces input distortions, voltage droop, and switching transients critical factors that can otherwise degrade timing margins and compromise carry accuracy in high-speed binary addition.

Performance Enhancement

Our technology enables the HD74LS83A to operate faster, more efficiently, and with improved precision, making it ideally suited for digital arithmetic applications that demand high-speed and accurate 4-bit binary addition.

Intel

The Intel Arria series is a family of mid-range FPGAs (Field-Programmable Gate Arrays) designed to balance performance, power efficiency, and cost. Positioned between Intel's high-end Stratix series and entry-level Cyclone series, Arria devices are widely used in applications such as communications infrastructure, industrial automation, broadcast, and aerospace. They offer features like high-speed transceivers, DSP blocks, and advanced logic capacity to support complex signal processing and data handling.

With the integration of efficient adders and arithmetic logic, Arria FPGAs are well-suited for accelerating workloads such as wireless baseband processing, video encoding/decoding, and data center acceleration, providing designers with flexible, reconfigurable hardware for performance-critical applications.

The Arria® 10 device family represents a class of high-performance, power-efficient 20 nm mid-range FPGAs and SoCs designed to meet modern computing demands. These devices deliver significantly higher performance compared to previous generations of mid-range and even high-end FPGAs, while incorporating advanced power-saving technologies that ensure optimal energy efficiency.

Arria® 10 FPGAs and SoC FPGAs deliver more than a full speed grade of core performance improvement and up to a 20% advantage in fMAX compared to the competition, based on publicly available OpenCore designs. They also offer up to 40% lower power consumption than previous-generation FPGAs and SoC FPGAs. With their combination of performance, power efficiency, and compact form factor, Arria® 10 devices are ideal for a broad range of applications, including communications, data center, military, broadcast, automotive, and other midrange FPGA use cases.

iv. WO2023220537A1 – Intel Arria 10 FPGA and Soc FPGAs

Value-Added Enhancements of WO2023220537A1 to Intel Arria 10 FPFA and Soc FPGAs

Enhanced DSP Performance

Arria 10 FPGAs are widely used for digital signal processing, where adders are central to arithmetic-heavy operations. By integrating our adder technology, these devices can achieve higher throughput in wireless communication, video processing, and real-time analytics, strengthening their DSP performance.

Low Power Consumption

Power efficiency is critical in networking and embedded systems. Our constant-gate-depth adder minimizes dynamic power use, making Arria 10 FPGAs more suitable for energy-sensitive applications without sacrificing performance.

Reduced Latency

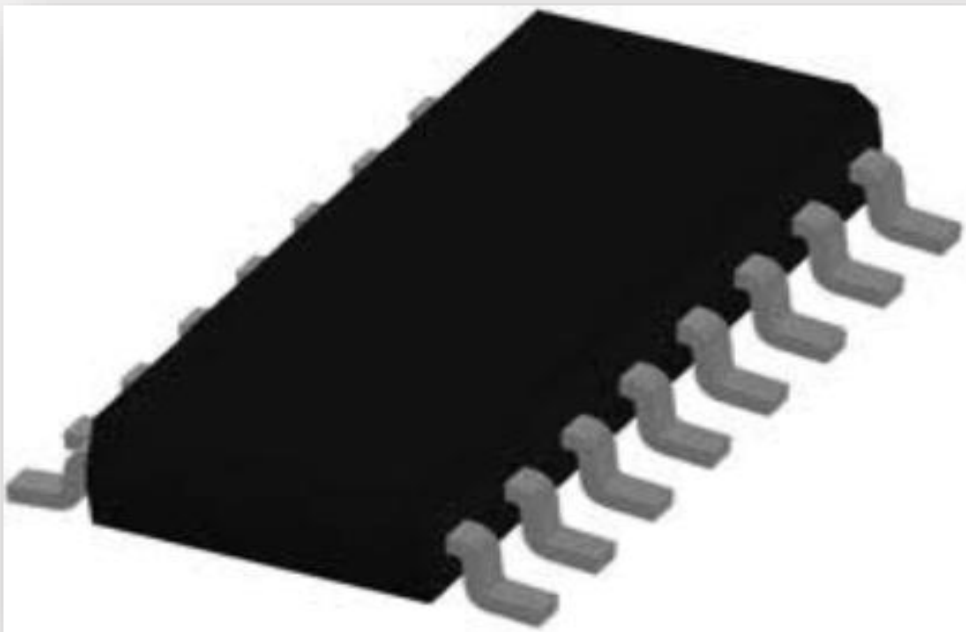
High-performance workloads like encryption, networking, and cloud acceleration demand low-latency arithmetic. With our adder, Arria 10 FPGAs can perform faster arithmetic operations, reducing delays and enabling real-time responsiveness.

Greater System Scalability

In SoC versions of the Arria 10, programmable logic is paired with ARM processors. Our adder enhances both sides of this architecture, allowing more complex, scalable designs that maintain efficiency in speed and power.

Onsemi

The MC14008B 4-bit full adder is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.



The MC14008B supports a wide supply voltage range from 3.0 V to 18 V, making it versatile for various power environments. It features diode protection on all inputs and buffered outputs, enhancing reliability and noise immunity. It is capable of driving two low-power TTL loads or one low-power Schottky TTL load throughout its rated temperature range, providing robust electrical performance.

Packaged in pin-for-pin replacement form factors compatible with the CD4008B, the MC14008B is available in Pb-free and RoHS-compliant packages, suitable for environmentally conscious designs. The device operates reliably in typical industrial temperature ranges and can be utilized within complex digital systems requiring swift and dependable addition with integrated carry look-ahead logic to reduce propagation delay.

This combination of wide voltage range, internal look-ahead carry, and robust input/output protections makes the MC14008B a dependable choice for high-performance digital and arithmetic systems requiring 4-bit binary addition.

v. WO2023220537A1- OnSemi MC14008B

Value-Added Enhancements of WO2023220537A1 to Onsemi MC14008B

Simplified Linear Adder Structure

Our technology introduces a simple linear approach to the adder design, streamlining the integration with the Onsemi MC14008B and reducing overall circuit complexity compared to traditional multi-stage logic implementations.

Technology Compatibility & Power Efficiency

The MC14008B utilizes P-channel and N-channel MOS enhancement-mode devices, and our technology aligns seamlessly with this architecture to boost performance while maintaining the device's low power profile.

Improved Signal Linearity & Reduced Distortion

The simple linear drive feature of our technology delivers a cleaner and more stable input signal, which effectively mitigates non-idealities such as input voltage droop, crossover distortion, and switching transients. This results in improved signal integrity and enhanced overall performance when interfaced with the MC14008B

Wide Supply Voltage Range

Operating over a wide supply voltage range from 3.0 V to 18 V, the MC14008B offers flexibility across various power environments. Our technology complements this versatility by ensuring reliable performance and consistent signal integrity throughout the entire operating range

AMD

AMD Radeon™ RX 9060 XT graphics cards are built to deliver all you need for ultra-fast gaming, with next-level visuals and future-ready features, supercharged with AI.

Built on the AMD RDNA™ 4 architecture, experience powerful raytracing and AI accelerators, increased visual quality for video streaming and recording, all backed by continuous optimizations with AMD Software.

Whether you need ultra-high refresh rates for esports, or all settings maxed for exploring your favorite open-worlds, AMD Radeon™ RX 9000 Series graphics deliver all you need for ultra-fast gaming. Supercharge your experience with AMD HYPR-RX[1] and unleash the true potential of your Radeon™ RX GPU, leveraging the combined forces of advanced super resolution, frame generation, and latency reduction technologies.

vi. WO2023220537A1 – AMD Radeon RX 9060 XT

Value-Added Enhancements of WO2023220537A1 to AMD Raedon RX 9060 XT

Enhanced Graphics Performance

By integrating our advanced adder technology, the RX 9060 XT can accelerate arithmetic-heavy operations within its shader and compute units. This leads to faster frame rendering, smoother gaming experiences, and higher efficiency in real-time ray tracing and complex visual effects.

Optimized AI and Compute Workloads

The RX 9060 XT already leverages parallelism for AI-driven graphics and upscaling technologies. With our technology, the GPU can handle matrix multiplications, convolution operations, and neural network inference more efficiently, resulting in superior AI-powered features.

Improved Power Efficiency

Our technology reduce switching activity and optimize critical paths, lowering the overall energy consumption of arithmetic operations. For the RX 9060 XT, this translates to delivering higher performance per watt, enabling longer gaming sessions and reduced cooling requirements while maintaining top-tier performance.

Faster ALU execution

Our technology enhances the efficiency of adder units within the RX 9060 XT's ALUs, reducing delay in arithmetic operations. This allows the GPU to execute more instructions per cycle, leading to faster rendering speeds and improved performance.

POTENTIAL LICENSEE

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AMD	ROBERT BOSCH	JAMECO ELECTRONICS
CRAY INC	SONY CORPORATION	TSMC
NVIDIA	HOLTEX SEMICONDUCTOR	ROCKWELL AUTOMATION
TEXAS INSTRUMENTS	SILICON LABS	SIEMENS AG
ARM	NUVOTON TECHNOLOGY	ADVANTECH
ON SEMICONDUCTOR	NORDIC SEMICONDUCTOR	ABB LTD
APPLIED MATERIALS	RASPBERRY PI	AXIOMTEK
IBM	ESPRESSIF SYSTEM	CEREBRAS SYSTEMS
MEDIATEK	PANASONIC	SAMBANOVA SYSTEMS
SK HYNIX	EPSON	GRAPHCORE
ANALOG DEVICES	MARVELL	CAMBRICON TECHNOLOGIES
APPLE	QUALCOMM TECHNOLOGIES	MATROX
AWS	CIRRUS LOGIC	NIVIS, LLC
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ASML	KRAMER	THALES
RENESAS ELECTRONICS	ACME CHIP	FUTUREX
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ADLINK TECHNOLOGY	VERISILICON	MENLO MICRO
OMRON	CRESTON ELECTRONICS	IAR SYSTEMS
4D SYSTEM	ASAHI KASEI MICRODEVICES	CICADA SEMICONDUCTOR
MICROCHIP TECHNOLOGY INC	FAIRCHILD SEMICONDUCTOR	MORPHO TECHNOLOGIES
MAXLINEAR	MITSUBISHI ELECTRICS	APHEX SYSTEMS
MICROSOFT	HITACHI	DSPACE GMBH
ROHM SEMICONDUCTOR	JINGJIA MICRO	SYMETRIX INC.
INFINEON TECHNOLOGIES AG	LANSDALE SEMICONDUCTORS	MIPS TECHNOLOGIES
NXP SEMICONDUCTOR	ASUS	INGENIC SEMICONDUCTOR
TOSHIBA ELECTRONICS	VIA TECHNOLOGIES	ZHAOXIN SEMICONDUCTOR

CONCLUSION:

The portfolio, comprising patents WO2023220537A1, CN119678130A, KR20250020455A, GB2634424A, JP2025522231A, CA3253057, SG11202407900T, US18864662, and IN202417097720, describes a foundational breakthrough in digital arithmetic: the Simple Linear Fast Adder (SLFA).

The SLFA is not merely an optimized circuit; it is a new paradigm for computation based on a Finite State Machine model of addition. Its architecture is uniquely defined by a natural one-to-one correspondence between memory and logic, making it an inherently Compute-in-Memory (CIM) system. This co-location of storage and computation directly mitigates the Von Neumann bottleneck, the primary source of energy waste in modern computing, at the algorithmic level, without depending on new materials and transistor types.

Acting as a Finite State Machine constructed from identical subunits connected in series—each containing only one AND gate, one XOR gate, and a two-bit register—the SLFA delivers a previously unattainable combination of benefits:

- Logarithmic average delay for high-speed performance.
- Constant gate depth and power dissipation for predictable, low-energy operation.
- Perfectly linear and scalable topology for easy design and manufacturing using standard CMOS processes.

This efficient, CIM-native core is scalable from a standalone arithmetic block to a tiled rectangular grid for parallel multi-input addition and matrix multiplication. It is therefore positioned as a transformative solution across the entire computing landscape, from low-power IoT and embedded systems to high-performance CPUs, AI accelerators, and the next generation of CIM architectures. The growing demand for high-speed, low-power computing in AI, data centers, and cryptography makes the efficient, scalable, and manufacturable SLFA not just a timely innovation, but a pivotal enabler of future technological progress.

2025

THANK-YOU

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