PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: JUAN PABLO RAMIREZ
#7100 131 ST ST.
PALOS HEIGHTS, IL 60463
US

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	SEP 28 2023

Applicant's or agent's file reference	FOR FURTHER ACTION
SLFA	See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2023/066525	02 May 2023	11 May 2022

International Patent Classification (IPC) or both national classification and IPC

IPC(8) - INV. - G06F 7/575; G06F 7/505 (2023.01)
ADD. - G06F 7/556; G06F 7/42 (2023.01)

CPC - INV. - G06F 7/575; G06F 7/505 (2023.08)
ADD. - G06F 7/556; G06F 7/42 (2023.08)

Applicant RAMIREZ, JUAN PABLO

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 Facsimile No. 571-273-8300	23 August 2023	Taina Matos PCT Helpdesk: 571-272-4300 Telephone No. 571-272-4300

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2023/066525

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed.

   b. ☐ furnished subsequent to the international filing date for the purposes of international search (Rule 13*ter*.1(a)),

      ☐ accompanied by a statement to the effect that the sequence listing does not go beyond the disclosure in the international application as filed.

4. ☐ With regard to any nucleotide and/or amino acid sequence disclosed in the international application, this opinion has been established to the extent that a meaningful opinion could be formed without a WIPO Standard ST.26 compliant sequence listing.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
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Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-15	YES
	Claims	None	NO
Inventive step (IS)	Claims	1-15	YES
	Claims	None	NO
Industrial applicability (IA)	Claims	1-15	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-15 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest:

Regarding claim 1, the prior art of record, individually or in combination, does not teach or fairly suggest a linear fast adder for an Arithmetic Logic Unit (ALU), the adder comprising: a) a four-bit adder component comprising a plurality of logic gates comprising at least sixteen AND gates, four XOR gates; and b) a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Claims 2-15 depend from claim 1, and therefore meet the criteria set out in PCT Article 33(2)-(3) for at least the same reasons as claim 1.

The prior art teaches some of the concepts and/or aspects of the claim limitations as shown below, but does not teach the claim limitations in their entirety and as specifically recited in each of the claims, nor would it have been obvious to one of ordinary skill in the art to combine the prior art references to achieve the claim in its entirety:

Freeman (US 4,377,807 A) teaches a four-bit adder comprising two AND gates (see Fig. 3, col. 3, lines 35-65, four-bit adder 60, with AND gates 94 & 98). Freeman fails to teach a four-bit adder component comprising a plurality of logic gates comprising at least sixteen AND gates, four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Flahie (US 5,912,832 A) teaches a 4 x 4 bit fast multiplier comprising a plurality of AND gates (see Fig. 14, col. 7, lines 1-50, 4 x 4 bit fast multiplier CHA, with 16 AND gates 104). Flahie fails to teach a four-bit adder component comprising at least four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Nagendra teaches linear fast adder (see Pages 2-3, which teach that logic circuits designed for speed, such as a 32 bit adder, are faster and more complex, and general consume more area and power). Nagendra also teaches that (CMOS technology reduces power dissipation, see pages 7-9). Nagendra also teaches a variety of gate depth configurations (see pages 10-11).
Nagendra fails to teach a four-bit adder component comprising at least 16 AND gates; four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Dungavath teaches a variety of configurations of high-speed, low power consumption adders (see Dungavath, pages 2-4, 7, 12-13, 18 & 24-26). Dungavath fails to teach a four-bit adder component comprising at least 16 AND gates; four XOR gates; a plurality of one-bit registers; wherein the four-bit adder is configured with a, linear area, linear complexity and a logarithmic delay; and wherein the four-bit adder has a constant gate depth thereby resulting in constant power dissipation.

Claims 1-15 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.