



## IP RISK ANALYSIS

FOR THE IMPLEMENTATION OF:

*A COMPUTE-IN-MEMORY ARITHMETIC CORE WITH  
**+85% EFFICIENCY AND THROUGHPUT GAINS**  
USING STANDARD CMOS TECHNOLOGY*

[www.binaryprojx.com](http://www.binaryprojx.com)

[ DIGITAL OPERATIONS AND ENCRYPTED DATA PROCESSING, SAS (MEXICO) ]

Addition is a deterministic algorithm, and **our Simple and Linear Fast Adder is a sequential circuit that is easy to understand and analyze**, and that executes a proven mathematical theorem. It is not a complex circuit with unpredictable behavior. Peer-reviewed proofs of its functional correctness and time-to-stability have been published. Aside from the theoretical foundations and mathematical algorithms published, the circuit logic, and RTL design have been detailed in numerous international conferences and peer-reviewed publications. **The proposed Compute-In-Memory (CIM) adder architecture is not contingent on new component technology or manufacturing processes.** It is completely achievable using standard CMOS transistors and memory cells, and is **generalized in rectangular arrays that can execute general operations such as matrix multiplication (operation behind AI, and graphics) and the 64-round compression function of SHA-256, among others.**

An international PCT patent application is currently in national phase in eight key jurisdictions: US, China, Japan, Korea, India, Singapore, UK, and Canada. **The patent has received a favorable written opinion from the International Searching Authority (USPTO) with all 15 claims approved without amendment**—a rare outcome indicating strong novelty and industrial applicability. **A third-party valuation from InTraCoM Group (Germany-based global patent valuation experts) places current value at +\$8 Million USD.** InTraCoM has extensive experience working with international blue-chip corporations, financial institutions, and technology-driven organizations, reinforcing the credibility and institutional rigor of this valuation. Additionally, we have a **comprehensive technology and market report (Patent Brokerage Report) from Anuation Research & Consulting LLP**, including a detailed market study that illustrates the practical usability of the product and demonstrates real-world applications of the underlying technology, which can be shared to support further evaluation and commercial understanding.

**We are positioned to initiate early-stage licensing discussions, while recognizing that building and benchmarking a prototype will significantly enhance both the value and commercial readiness of the IP.** Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type. That performance is what we will benchmark via FPGA emulation of the RTL design. **We can infer and project performance and efficiency gains, based on other Compute-In-Memory architectures that cut out similar data movement**, although they cut out data movement through other means (experimental transistor types; segmenting subunits and relocating them; super-specific ASIC designs). **The main differences between our CIM arithmetic core and other CIM schemes are the time-to-market, universality of applicability, and R+D costs.**

# Index

"SLFA" International Patent Brief.....	4
Solid Patent Standing.....	4
Technical Feasibility.....	4
Valuation and Market Strategy.....	4
Risk Analysis.....	5
IP Risk.....	5
Broad and Defensible Coverage.....	5
Faster Time-to-Grant.....	5
Summary.....	6
Reccomended Action.....	6
Final Assesment.....	7
Thank You.....	8

# "SLFA" International Patent Brief

## 1. SOLID PATENT STANDING

- Filed via USPTO (ISA) with a favorable written opinion.
- All 15 claims passed without amendment — which is highly unusual and speaks to strong novelty, inventiveness, and industrial applicability. This means the entire core and scope of the invention is both valid and enforceable. It is also very rare for all claims to be accepted without amendment and speaks of a solid IP coverage.
  - **Novel:** The design is not disclosed in any prior art globally.
  - **Inventive:** The design is not an obvious variation of known circuits.
  - **Industrial Applicability:** It can be implemented with current technology (FPGAs/ASICs).
- National phase entered in all key markets (U.S., China, Japan, Korea, UK, Singapore, India, and Canada), backed by the Indian IP firm Anuation — indicating professional prosecution and global strategy.

## 2. TECHNICAL FEASIBILITY

The next two years are about further **de-risking the technology at a physical level and creating the licensable asset** (GDSII tape-out ready Stream File), with a **Pre-Seed investment of \$6.6 Million USD**. Our cash burn-rate will be primarily driven by the engineering team's salaries, signing bonuses, tools, and resources. This investment is divided into two stages.

- Patent describes a simple, linear adder implementable with existing transistor and memory tech — no exotic materials or experimental physics.
- Development Plan ready for prototyping using FPGA, and a standard path toward ASIC validation.
- The implementation can be integrated into mining ASICs in the form of a Compute-In-Memory HASH Engine.

## 3. VALUATION AND MARKET STRATEGY

- Third-party valuation from Intracom (Germany) places the **patent's current value at \$8 Million USD**, passing through experts who have vetted the invention. The value will increase during 2026, as the selected jurisdictions approve the application (national phase entered in May 2025), and we move to prototype.
- We´re offering a lifetime stake in a mining operation that will use the ASICs we design, acquired from licensing our design to existing ASIC manufacturers.

# RISK ANALYSIS

## 1. IP RISK

- You're not betting on uncertain patentability.
- The IP asset is already legally sound across all 15 claims.
- Strong position if licensing, defending, or commercializing.

## 2. BROAD AND DEFENSIBLE COVERAGE

- Multiple claims cover variants of the design — pipeline versions, reduced power modes, different versions, etc.
- If granted as-is in national phases, this will give wide protection from competitors trying to “design around” the core idea.

## 3. FASTER TIME TO GRANT

- You're not betting on uncertain patentability.
- The IP asset is already legally sound across all 15 claims.
- Strong position if licensing, defending, or commercializing.

## RECOMMENDED ACTION

Since the ISA outcome is this positive, you're in a strong position to:

- Secure an agreement with robust IP clauses (e.g., licensing scope, royalty floor, profit-sharing from ASIC sales/mining).
- Request a copy of the ISR and WO/ISA Written Opinion for your records and due binder.
- Verify national phase entries (should match filing data in U.S., China, Japan, etc.)— all reflect the same unamended claims.
- Strong position if licensing, defending, or commercializing.

## SUMMARY

This is a technically sound, legally strong, and implementation-ready IP asset — with a favorable international search report from the USPTO and zero required amendments. Low-IP-risk, Low-tech-risk, high-upside opportunity.

- Strong IP
- Practical tech
- Global patent coverage
- Defined ROI model
- A motivated team with real progress made

# Final Assessment

## CATEGORY

<b>Patent Quality</b>	High — 15 unamended claims approved by USPTO-ISA, national phase entered in key jurisdictions, managed by professional IP firm (Anuation).
<b>Technical Risk</b>	Moderate to Low — FPGA emulation planned, design based on standard logic and compatible with existing semiconductor processes.
<b>Implementation Readiness</b>	Solid — Roadmap in place, no exotic materials or speculative components, investor handles mining ops.
<b>IP Risk</b>	Very Low — Favorable international search opinion, broad scope, legally defensible.
<b>Market Strategy</b>	Clear — Patent monetization through licensing and direct application in mining ASICs
<b>Investor Leverage</b>	High — Investment secures rights and a 20% stake in revenue-generating operations.
<b>Third-Party Valuation</b>	Intracom (Germany) values IP at \$8M — supports credibility and future exit potential.

This is a low-IP-risk, low-tech-risk, high-upside opportunity with well-structured patent coverage, and a clear path to implementation. Assuming milestones are met (FPGA emulation, roadmap compliance, licensing terms), this proposal is strategically aligned for investment.



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**THANK YOU!**

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