ARRAY

PITCH DECK

FOR THE IMPLEMENTATION OF:

A COMPUTE-IN-MEMORY ARITHMETIC CORE WITH
+85% EFFICIENCY AND THROUGHPUT GAINS
USING STANDARD CMOS TECHNOLOGY

www.fastarithmeticunits-dataroom.com

[DIGITAL OPERATIONS AND ENCRYPTED DATA PROCESSING, SAS (MEXICO)]

This FAQ provides a **summarized overview of our Compute-in-Memory Fast Arithmetic Unit (FAU)** technology. It outlines the **computing energy-wall** our innovation addresses, details our patented Simple and Linear Fast Adder (SLFA) architecture, and explains why our solution has the **potential to achieve significant processor efficiency and performance gains** using standard CMOS technology.

The document also covers our **IP protection status ($8M+ valuation, PCT national phase entry),** the 16-month development **roadmap to a tapeout-ready GDSII file,** our $6.6M seed funding request, market opportunity across **$540 Billion Dollar TAM,** as well as our first go-to-market **strategy focused on Bitcoin mining ASICs and AI** with expansion into cryptography, and graphics processing.

- ***The Problem:*** Parallel adders are complex, power-hungry units. Furthermore, data movement between memory arrays and arithmetic units consumes +95% of energy.

- ***The Breakthrough:*** A new definition of addition based on a finite-state machine. Two inputs transform in-place.

- ***The Architecture:*** Two Flip Flop columns. One Half Adder column. Bidirectional feedback. Perfect Manhattan grid. Standard CMOS.

- ***The Proof:*** IEEE-published. Peer-reviewed. SHA-256 compression function executed entirely in-situ. Independently valued.

- ***The Market:*** Bitcoin Mining ASICs. AI Accelerators. Cryptography. Edge computing. Digital Signal Processing.

- ***The Ask:*** US $500k for Pre Seed to validate and benchmark arithmetic core, and US $6. million Seed investment for a fully functional Compute-In-Memory Engine ready to be integrated into leading ASIC designs.

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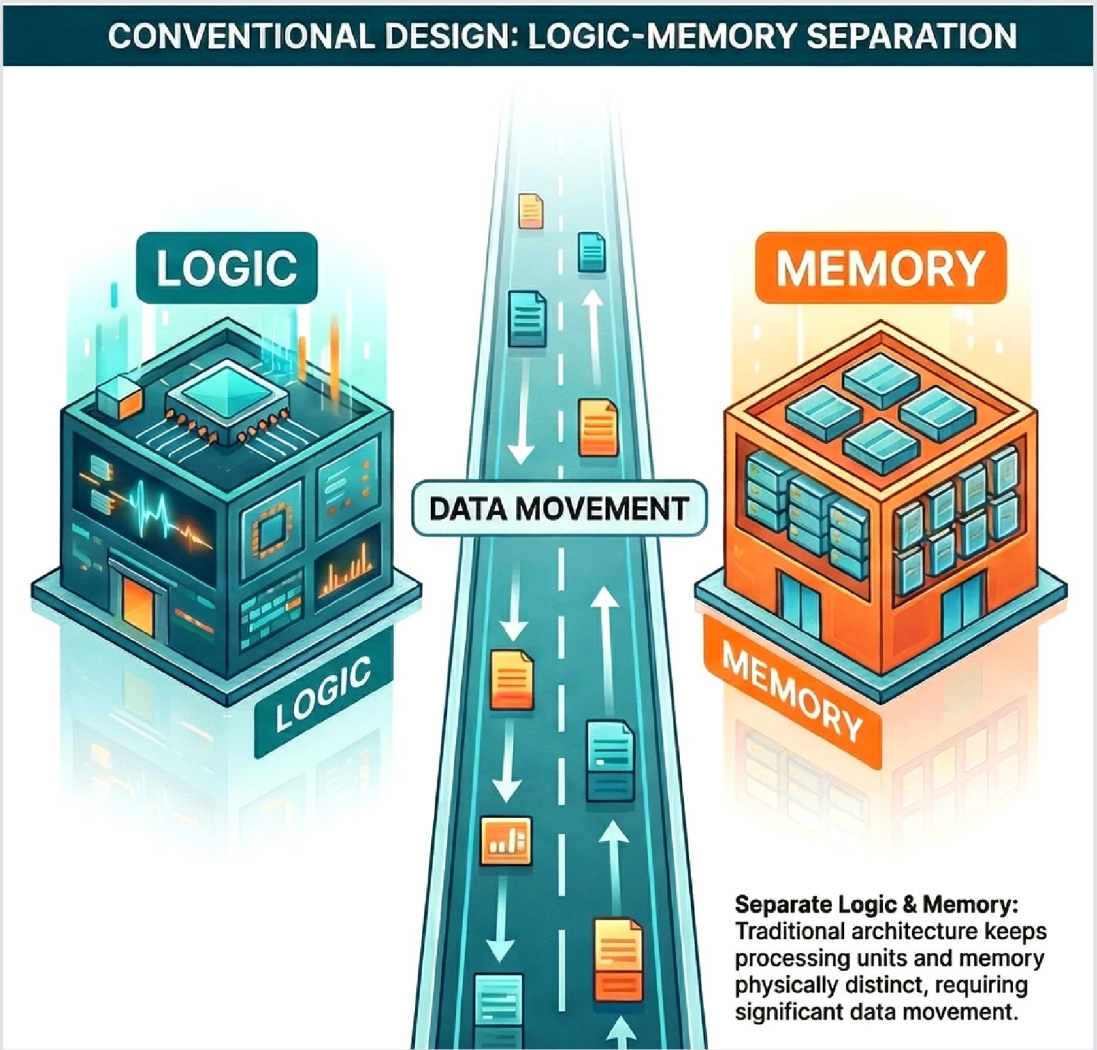
1. PROBLEM AND OPPORTUNITY STATEMENT

- The Arithmetic Logic Unit (ALU) is the most important part of any processor, given it is responsible for executing all the mathematical/logical operations (by far the most common operations in a processor).

- State-of-the-art Parallel Adders are not fast enough for modern applications and they are complex, unscalable and power-hungry circuits **and come with fundamental efficiency and performance trade-offs.**

- The 80-year-old Von Neumann architecture is fundamentally inefficient, **wasting 60-90% of time and energy just moving data** between memory arrays and arithmetic units of the processor. **Moving the data consumes over 100x more energy than the computation itself.** This ''Von Neumann Bottleneck'' costs billions and limits progress across industries.

- **Total Addressable Market (TAM) of $540 Billion dollars** in annual spending on microprocessors across several industries.



2. PRODUCT, SOLUTION, SERVICE OFFERING

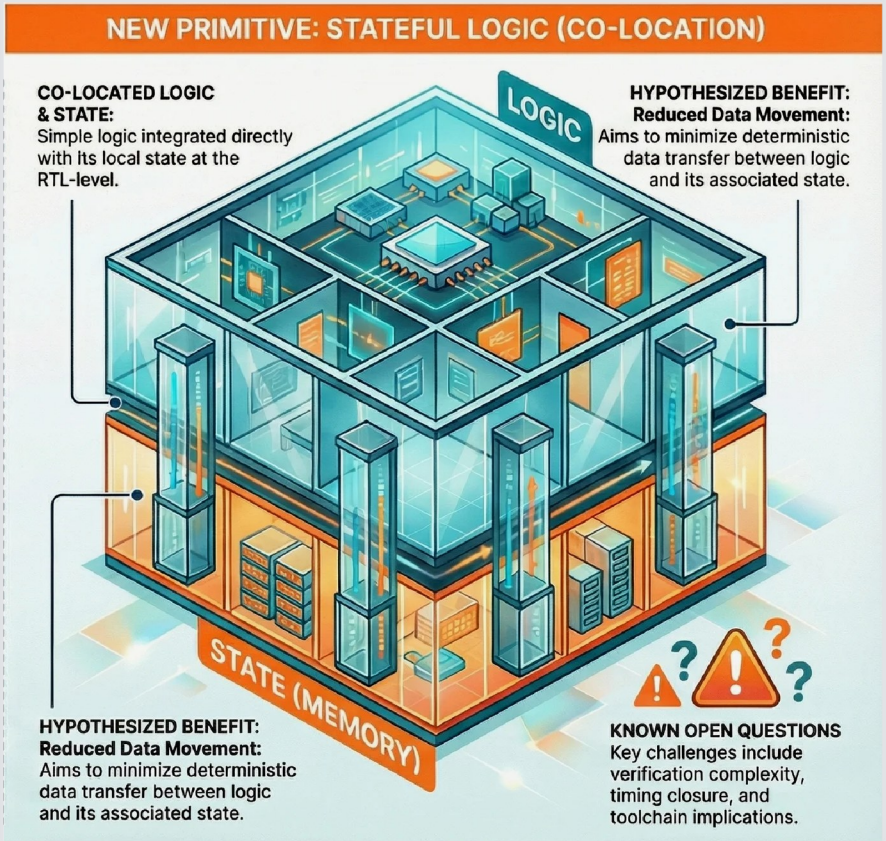
Our design solves major issues for **In-Memory Computing, enabling faster and cheaper (low-powered) In-Situ operations.** This perfect array of rows and columns performs fast addition and multiplication of multiple inputs, scalable for **optimized area and data movement** in hashing, matrix multiplication, and other arithmetic-intensive operations. Our architecture uses **current manufacturing standards and transistor types** to exploit an innovative arithmetic framework with **minimal R&D investment.**

- **Product:** Our licensable IP, the Fast Arithmetic Unit (FAU), is a novel design for **an arithmetic core that embeds logic and memory into a single rectangular array.** Unlike other Compute-In-Memory concepts that require new materials, **our FAU uses only standard transistors and processes.**

- **How it Works:** It is a fundamentally new definition of addition, implementable in a simple, linear, scalable design for general-purpose and area-specific arithmetic cores across a wide range of industries. The adder operates through **localized interactions between storage and computation, eliminating long-distance, energy-intensive data movement.**

- **The Deliverable:** We will deliver a tapeout-ready GDSII stream file—**a complete, verified blueprint for a Bitcoin Mining Engine**, **or AI Processor Cores.**

Among other case uses, the Simple and Linear Fast Adder can serve as the elemental building block for a **32-bit grid for in-memory execution of the 64-round SHA-256 compression function, which constitutes over 90% of Bitcoin mining's computational workload.** Data movement is restricted inside the grid, moving only between columns. The strictly regular, Manhattan-routed grid yields **predictable wire lengths and minimal routing congestion, enabling higher clock frequencies and lower operating voltages—saving energy per hash.**



Our architecture addresses a foundational inefficiency in the computing stack by reducing data movement, unlocking significant energy savings across data centers and compute-intensive applications.

BROADER ECOSYSTEM IMPACT

MULTIPLYING IMPACT

FOUNDATIONAL IMPACT

5. GLOBAL IMPACT

SUSTAINABILITY & SCALE

Lower energy demand reduces carbon footprint and enables sustainable scaling of AI and compute-driven industries.

GIGATON-LEVEL CO_2 REDUCTION

4. DATA CENTERS

INFRASTRUCTURE EFFICIENCY

Lower server power usage reduces cooling, power delivery, and space requirements across entire data centers.

10–30%
LESS DATA CENTER ENERGY

3. SYSTEM & SERVER

SYSTEM-LEVEL SAVINGS

Lower chip power enables more performance per watt and reduces total system power consumption.

20–50%
LESS SERVER POWER

2. CHIP / SILICON

CHIP EFFICIENCY

Our architecture reduces data movement between memory and logic—the most energy-intensive operation in computing.

50–90%
LESS ENERGY PER OPERATION

1. OUR ARCHITECTURE

ARRAY

FOUNDATIONAL INNOVATION

Compute-in-Memory architecture eliminates unnecessary data movement by performing operations where data resides.

DRAMATIC REDUCTION IN DATA MOVEMENT

THE COMPOUNDING BENEFIT

Small savings at the silicon level compound into massive impact at global scale.

= TRANSFORMING THE ENERGY ECONOMICS OF COMPUTING

LESS DATA MOVEMENT. LOWER ENERGY. GREATER IMPACT.

3. ALTERNATIVE TECHNOLOGIES AND COMPETITORS

Solutions and alternatives to the memory bottleneck exist (Compute-Near-Memory, High-Bandwidth Memory, Neuromorphic Computing, Compute-In-Memory, etc.), **but our competitors are optimizing within the Carry-Over paradigm of addition,** trying to solve the bottleneck problem with expensive new materials and processes, or specialized application-specific hardware.

- **Near-Memory Computing (NMC) and ASIC Design:** NeuralBlade, NVIDIA (High-Bandwidth Memory), AMD (Infinity Fabric), Intel (Optane), Samsung, Etched, MemComputing, MythicAI, Cerbras, etc.
- **Processing-in-Memory (PIM):** Samsung, SK Hynix, Micron, UMC, IBM.
- **Neuromorphic Computing:** Intel (Loihi), IBM (North Pole), BrainChip, SynSense, research centers such as Human Brain Project (EU).
- **Optical / Photonic Computing:** Lightmatter, Lightelligence, PsiQuantum, Xanadu, MIT CSAIL, NVIDIA.
- **Quantum Computing:** IBM Quantum, Google Quantum AI, IonQ, Rigetti Computing, D-Wave, Microsoft Quantum.

These approaches are not commercially viable due to massive R&D costs. For example, over the last decade **IBM, Intel and Samsung have each spent between $500 Million and $1 Billion USD** searching for more efficient computing architectures, based on new transistor technology which requires new fabs and processes.

Other market-ready options have **extremely limited applicability and market share** because they are specialized accelerators hardwired for very specific workloads (example of this include **Mythic AI, Cerebras, MemComputing, Neuroblade, Etched).**

4. DIFFERENTIATED TECHNOLOGY AND IP PROTECTION

The industry is currently trapped in a cycle of over-funding research on experimental transistor types, segmenting subunits and relocating them, and designing super-specific ASICs. We have solved the fundamental problem by redefining the algorithm for addition. We did not improve adder design by making it faster or better, we replaced the mathematical algorithm. **The main differences, between our FAU and other Compute-In-Memory schemes, are the time-to-market, universality of applicability, and R+D costs.** Our FAU combines scalability with the performance of state-of-the-art parallel adders and can be implemented across several key industries, all while being manufacturable with current CMOS technology.

The IP Risk is exceptionally low giving us a strong position for licensing, defending, or commercializing. The International Searching Authority **(USPTO) found all 15 claims to meet the 3 Patentability Criteria (Novel, Inventive, Industrially Applicable) without amendment** and has provided a very favorable Written Opinion. The patent application is in the national phase in key jurisdictions: US, China, Japan, Korea, India, Singapore, UK, and Canada. **A third-party valuation from InTraCoM Group (global patent valuation experts based in Germany) places current value at +$8 Million USD.** InTraCoM has extensive experience working with international blue-chip corporations, financial institutions, and technology-driven organizations, reinforcing the credibility and institutional rigor of this valuation. A technology/market report from Anuation Research & Consulting LLP (a leading IP & research firm) is also available.

	Traditional Adder Architecture		Non Von Neumann Architectures			
	Ripple Carry-Over (1st Gen)	**Parallel** (Carry-Look Ahead, Carry-Save, Kogge-Stone, etc.)	**Near-Memory Computing**	**Compute-In-Memory Transistor Arrays** (FeFETs, MRAM, ReRAM, etc.)	**ASIC** (On-Chip Pipelines)	**Simple and Linear Fast Adder** (Bit-Level Embedded Logic & Memory)
Competitors	Low-Power Systems Texas Instruments	Traditional Processors Intel, Nvidia, IBM, AMD, etc.	NeuroBlade, Nvidia, MythicAI	IBM, Intel, Samsung, SK Hynix, MythicAI	BitMain, Etched, Nvidia, Cerebras, NeuroBlade	Our IP
Energy (Efficiency)	◐	○	●	●	●	●
Time (Latency)	○	◐	●	●	●	●
Manufacturing (Costs and Requirements)	●	◐	◐	○	◐	●
Technology (R&D)	●	●	◐	○	◐	●
Applicability (Use Cases)	◐	●	◐	◐	◐	●
Scalability (Bit Length)	●	◐	◐	◐	◐	●

5. FEASIBILITY AND PROTOTYPE DEMONSTRATIONS

Addition is a deterministic algorithm, and our Simple and Linear Fast Adder **(SLFA) is a sequential circuit that executes a proven mathematical theorem. It is not a complex design with unpredictable behavior.** Peer-reviewed proofs of its functional correctness and time-to-stability have been published, and the circuit logic and RTL design have been detailed in numerous international conferences and publications. Furthermore, **the architecture requires no new components or manufacturing processes; it is fully realizable with standard CMOS transistors and memory cells.** Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type. We will anser this question through rigorous FPGA emulation of the RTL design.

Although we are ready to begin licensing immediately, **every de-risking step—such as FPGA emulation and benchmarking—significantly increases the IP's valuation.** The first phase is to verify and benchmark the arithmetic core, moving from validated IP to proven performance data. The prototype arithmetic core will then be integrated into a Bitcoin Mining Engine or AI Accelerator, in the second phase.

- We have moved from foundational mathematics to preliminary RTL design, awaiting silicon validation. **The core algorithm that is the subject of our IP portfolio has been peer-reviewed at the mathematical, algorithmic, and RTL Design level.**

- **16-Month De-risking Plan (RTL to GDSII Flow):** With funding, we will execute a clear 2-stage plan to deliver the licensable GDSII asset:

    - **Stage I (Months 1-6):** Prototype Arithmetic Core – FPGA emulation and benchmarking of the 32-bit Simple and Linear Fast Adder.

    - **Stage II**
        - **(Months 7-12):** Integration to ASIC Design Standards – Emulate and benchmark a SHA-256 Hashing core.
        - **(Months 13-16):** Integration to Manufacturing Standards – Produce the final, tapeout-ready GDSII files.

- We will use **industry-standard tools** (Synopsys, Cadence) for verification and **high-performance FPGAs** for emulation, and providing credible benchmarks. The main challenge in terms of implementation is to **expand our arithmetic core into a fully functional SHA-256 Hashing pipeline ready for integration into a System-on-Chip mining architecture.** This includes integration to the surrounding infrastructure for the core: control logic, memory blocks, data movement, and I/O to create a functional system.

Technology Readiness Level (TRL-3): From Math Theory, to Licensable IP, to SoC

Completed
(Founder Funded)

First Stage
Investment-
6 Months
$500K USD

Second Stage
Investment-
10 Months
$6.1 Million USD

Hand-Over/Joint Development
Licensing Revenue

TRL	Definition	Exit Criteria
1	Basic principles observed and reported.	Peer reviewed publication of research underlying the proposed concept/application. **(Peer-reviewed Publications, International Conferences, etc).**
2	Technology concept and/or application formulated.	Documented description of the application/concept that addresses feasibility and benefit. **(Patent Application, Valuation, and Market Report).**
3	Analytical and experimental critical function and/or characteristic proof of concept.	Documented analytical/experimental results validating predictions of key parameters.
4	Component and/or breadboard validation in laboratory environment.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of relevant environment.
5	Component and/or breadboard validation in relevant environment.	Documented test performance demonstrating agreement with analytical predictions. Documented definition of scaling requirements.
6	System/sub-system model or prototype demonstration in an operational environment.	Documented test performance demonstrating agreement with analytical predictions.
7	System prototype demonstration in an operational environment.	Documented test performance demonstrating agreement with analytical predictions.
8	Actual system completed and "flight qualified" through test and demonstration.	Documented test performance verifying analytical predictions.
9	Actual system flight proven through successful mission operations.	Documented operational results.

6. FUNDING AMOUNT AND TIMELINE

The next two years are about further **de-risking the technology at a physical level and creating the licensable asset** (GDSII tape-out ready Stream File), with a **an investment of $6.6 MIllion USD.** Our cash burn-rate will be primarily driven by the engineering team's salaries, signing bonuses, tools, and resources. This investment is divided into two stages.

1. **With $500k Pre-Seed Funding (6-8 months)** we will deliver a fully verified RTL implementation of our CIM Adder. **FPGA emulation and benchmarking completely increases the value of our underlying IP portfolio.** The deliverables for this first stage are lab verified RTL, simulation models, and performance data. It proves our 30-40% efficiency gains and positions us for a larger Series A.
2. **With $6.1 Million in Seed Funding (10 months)** we will build-up a world-class nine-person team to deliver a complete, tapeout-ready SoC design for executing either matrix multiplication (AI/GPUs) or the 64-round compression function of SHA-256 (Bitcoin mining). This 10 month stage results in a manufacturable prototype ASIC. This is an immediately licensable asset for semiconductor companies.

Use of Funds: This is not just for R&D, it is also primarily for team building.

- 47%: Technical Team Salaries & Signing Bonuses (attract top talent).
- 21%: Tools, Resources, Workspace (FPGAs, EDA Suites, lab).
- 15%: Legal, Fiscal, IP, and Administration.
- 17%: Contingency Fund.

Year 1: ~60%

- Consolidation of working capital
- Arithmetic Core RTL Design
- Integration to ASIC Design Standards

Year 2: ~25%

- Physical Design and Integration to ASIC Manufacturing Standards.

Previous Funding: Research, Conferences, Papers, and IP protection have all been founder-funded to date.

Team and Key Technical Hires (2 Year Salaries and Signing Bonuses): $3.75 Million USD

- ***Senior Engineers (3): $1 Million USD***
  - (1) Senior ASIC Physical Design Engineer (Senior Staff Engineer)
  - (1) Senior ASIC Design Engineer
  - (1) Senior Verification Engineer
- ***Junior Engineers (4): $800,000 USD***
  - (2) RTL to Pre-Silicon Design Engineers (2)
  - (2) FPGA/Verification Engineers (2)
- ***Environment & Infrastructure Setup, Maintenance, and Support (2): $300,000 USD***
  - (1) Senior CAD Flow Engineer
  - (1) Script & Lab Building Engineer
- ***Talent Acquisition, Signing and Relocation Bonuses, Recruiting Agency Fees: $1 Million USD***
- ***Core Team: $650,000 USD***
  - Lead Architect and Project Manager (Founder)
  - Administrative Management

- **Tools & Resources: $1.4 Million USD**
  - ***Workstations: $75,000 USD***
    - Main Server
    - Team 1 Workstation (WS 1)
    - Team 2 Workstation (WS 2)
    - Sr. Staff Engineer Workstation (WS 3)
    - Remote Workstations for Sr. Engineers (4)
  - ***Hardware: $85,000 USD***
    - FPGA Kits
    - Virtex 7 (2)
    - Alveo U55C
    - Alveo V80
    - Lab Instrumentation
  - ***Licensed EDA Software: $1,000,000 USD***
    - Vivado Design Suite
    - Cadence Design Suite
    - Synopsys Design Compiler and VCS
    - Siemens Veloce
    - Ansys RedHawk

- **Workspace for 15 persons in Guadalajara Metropolitan Area: $250,000 USD**
  - Two years of office rent
  - Basic office equipment

- **International Conferences & Publications: $20,000 USD**

- **Collaboration with University of Guadalajara: $30,000 USD**
  - Graduate Students
  - Lab Hours, Workspace, and PCB Equipment

- **Marketing and Placement Agencies, Commercial Department: $300,000 USD**

SUBTOTAL: $5.5 Million USD
Contingency Fund: $1’100,000 USD (+20%)

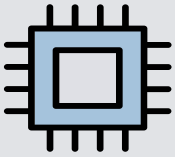
TOTAL: $6.6 Million USD

7. MILESTONES AND DELIVERABLES FOR NEXT 24 MONTHS AND BEYOND

6-Month Milestone

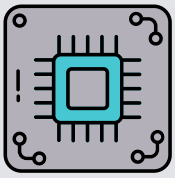
Verified and Benchmarked Arithmetic Core

12-Month Milestone



Complete RTL design of ASIC Processor

16-Month Milestone



Silicon-Ready GDSII Stream File

Licensing Revenue

Revenue from Commercial License Agreements

8. MARKET AND CUSTOMERS

The annual consumption of microprocessors in our Total Addressable Market is approximately $540 Billion USD. More than 150 potential licensees have been identified in a third-party market report.

- **TAM:** $540B (All Microprocessors)
- **SAM:** $60B (Mining ASICs)
- **SOM:** $600M (1% of SAM)

Primary Customers: We will first target the **Bitcoin mining ASIC market** with area and energy-efficient hashing cores. Initial licensees include ASIC design firms, manufacturers, and foundries. We have a clear path to a licensing model that boosts their product performance with minimal risk.

- Our chips **remain profitable during price dips.**
- Our customers **survive bear markets** competitors don't.
- We **control the mining efficiency curve** for years.

Future Markets: This is a platform technology. We will later target AI/ML (Multiply-Accumulate Circuits), graphics rendering, cryptography hardware, and Digital Signal Processing.

Artificial Intelligence — $200BUSD/year in MP

Matrix multiplication is the core operation of neural networks. It directly affects the training speed and scalability of AI models.

Graphics and Gaming — $100BUSD/year in MP

Transformations like rotation, scaling, and translation in 3D graphics rely on matrix operations.

Blockchain and Bitcoin Mining — $60BUSD/year in MP

Matrix multiplication is fundamental to many cryptographic algorithms used for secure key exchange, encryption, and decryption.

Digital Signal Processing — $40BUSD/year in MP

DSP for audio, image, and video data relies on matrix multiplication for tasks like imaging, filtering, coordinate transformations, and data compression.

Data Analysis and Big Data — $60BUSD/year in MP

Principal Component Analysis (PCA) and ML models leverage matrix multiplication to analyze correlations and patterns in massive datasets.

Cryptography and Security — $30BUSD/year in MP

Matrix multiplication is fundamental to cryptographic algorithms used for securing sensitive data, especially in real-time applications.

9. BUSINESS AND GO-TO-MARKET MODEL

Our business model is **IP Licensing with revenue from upfront Licensing Fees, Royalties.**

Model: IP Licensing & Co-Design.

Revenue Streams

- **Upfront Licensing Fees:** From world leading ASIC design and manufacturing companies.
- **Income Royalties:** Fixed percetage from total sales revenue from product lines stemming from our IP technology.
- **In-Kind Royalties:** Manufacturing Shares of 1-3% of mining ASICs manufactured with our IP, to setup our own mining operation.

10. PARTNERSHIPS (CURRENT AND DESIRED)

Current: We have a collaborative relationship with the University of Guadalajara, giving us access to graduate talent, and lab hours, and we are also working with Base Layer Advisors.

Desired: We seek additional partnerships with:

- ASIC Manufacturers (as licensees and for joint development).
- Mining Pools/Farms (as first customers and validators).
- VCs and Angels with deep-tech/semiconductor networks to help us build a world-class team.

11. EXIT STRATEGY

Our primary strategy is to build a profitable, high-margin, self-sustaining IP licensing firm, generating recurring revenue from a broad portfolio of licensees.

12. FINANCIAL PROJECTIONS

- We seek to consolidate as a design firm for **next-generation high-performance area-specific processor arithmetic cores,** with a vested interest in the design, manufacture and operation of Bitcoin mining ASICs.

- Our Simple and Linear Fast Adder (SLFA) architecture executes arithmetic inside memory, and promises **30-40% increase** in Bitcoin Mining ASIC performance and efficiency, translating directly to a **75-100% increase in bottom-line profits.**

- We estimate an **annual revenue of $210 Million USD and $165 Million USD profits operating just 30K CIM mining ASICs** through our hybrid licensing/mining revenue model under a conservative scenario, considering the following variable values:

    - **License Fee:**
        - *Licenses Placed:* 3 Licenses.
        - *Non-Exclusive Right-of-Use License:* **$5 Million USD per Year (upfront fee).**
        - *Minimum Contract Period:* 5 Years.

    - **Royalties:** Close to 80% of our projected revenue will come in the form of Bitcoin mined with ASICs we will receive as **in-kind royalties from licensing to manufacturers.**

13. FOUNDERS, EXECUTIVES, AND KEY STAFF

Architect, Founder & CEO: Juan Pablo Ramírez
More than 12 years of R&D leading to the patented FAU. Published author in mathematics and computer science.

Co-Founder & CFO: Pablo César Vázquez Estrella
Head of Finance and Buisiness Strategy, Investor Relations and Corporate Development.

Senior Software Engineer: Sergio Adrián Trujillo González
Software environments and scripting.

Elec. Eng. Consultant, University of Guadalajara: Héctor Alejandro Galvez López
Our link to the University of Guadalajara, providing access to talent and lab resources.

The Gap We Are Filling: The $6.6 Million seed round is primarily to recruit a world-class team led by a Senior ASIC Physical Design Engineer.

14. CORPORATE INFORMATION

Company Name: Digital Operations and Encrypted Data Processing, SAS.

Incorporated in: Guadalajara, Mexico (Known as Mexico's Silicon Valley).

Advisors/Board: Currently, the founding team, and Base Layer Advisors LLC. We are actively seeking to build an advisory board with semiconductor industry veterans.

Global IP protection and patent portfolio management: Anuation Research & Consulting LLP.

CAP TABLE

Founder	**80%**
Co-Founder	**15%**
Key Staff	**5%**

15. HIGH PRIORITY NEEDS OVER NEXT 24 MONTHS

Our detailed development plan identifies **four high-priority needs where venture capital and strategic partnering will help de-risk and ensure our success.**

- **Strategic Capital:** The **$6.6 Million** to execute the development plan.

- **Recruitment Network:** A solid network is our top recruitment engine. Warm introductions to companies and partners in the semiconductor space are essential to attract the world-class Senior ASIC Physical Design Manager and Engineers this project requires.

- **In-Kind Services:** Access to EDA tools (Cadence, Synopsys) would significantly reduce our operational costs.

- **Mentorship & Guidance:** Strategic advice on navigating the semiconductor manufacturing landscape and making introductions to potential licensees in your network.

16. RISKS AND GAPS

Execution Risk (The Biggest Risk): Building a world-class team from scratch. *Mitigation:* We require top-tier recruiters and the active use of our investors' networks—exactly why a strategic partnership is so critical. These introductions would be the single biggest accelerant and de-risking action.

Technical Risk: The architecture could require late stage corrections. *Mitigation:* Our 3-stage plan with rigorous FPGA emulation and benchmarking at each stage de-risks this progressively. The underlying mathematics and early design have been peer-reviewed and presented at international conferences.

Market Risk: Bitcoin and Crypto mining is our first approach, but it can be a volatile market. *Mitigation:* Our IP is a platform technology, applicable to AI and other large, stable markets, providing a natural pivot if needed.

IP Risk: Patent challenges. *Mitigation:* A patent application is currently in the **national phase in key jurisdictions:** US, China, Japan, Korea, India, Singapore, UK, and Canada. A **third-party valuation from InTraCoM Group (global patent valuation experts based in Germany) places current value at +$8 Million USD,** and a technology/market report from Anuation Research & Consulting LLP (a leading IP & research firm) is available.

The Hard Questions

"If this is so simple, why hasn't anyone done it before?"
For decades the industry has optimized the carry-propagation algorithm, not replaced it. This takes a mathematician redefining addition from first principles because it is a domain outside conventional digital design. Although easy to understand, the solution is counterintuitive to engineers trained in the carry-chain paradigm.

"Is this analog? What about noise and process variation?"
Fully digital. Standard CMOS logic. No interpreting analog current levels or probabilistic error correction. It behaves exactly like any standard digital block in any CMOS library. No exotic design, principles, materials or components.

"Can't a big player just copy this?"
While the Two-Input Adder is a valuable asset, the real value and industrial applicability comes from scaling into a Multiple-Input Adder. This is not a trivial jump, but we have matured the underlying designs in-house, giving us a long head-start. Furthermore, we do not seek to compete, rather license our IP arithmetic cores to design houses and manufacturers. That is a stronger moat than a circuit patent. Additionally, the architecture is non-obvious to engineers entrenched in traditional adder design. More than half a century of carry-propagate thinking is our best defence.

"What stops them from designing around it?"
The algorithm is the addition operation. To add two numbers without our design, you must revert to some form of Carry-Propagation paradigm of addition. There is no third way. We have protected the only alternative.

"Where's the silicon?"
We have peer-reviewed and published RTL and logic synthesis which is the first step in taking any prototype to Silicon. The Pre-Seed round is to verify and benchmark an emulated arithmetic core — moving from validated IP to proven performance data. The Seed round is for integrating the arithmetic core into a fully functional System-on-Chip Bitcoin Mining Engine or AI Accelerator. Probability of success is therefore not a matter of 'if it works, but of 'how well it performs' in a given process node and ASIC type.

"What's the real power/performance advantage? Give me a number."
For a 32-bit addition: logarithmic average iterations (≈5), constant gate depth per iteration, and zero data-movement energy. That eliminates most of the energy cost attributed to memory-to-ALU data transfer whcih is the main driver in power consumption and time.latency. We will deliver exact normalized metrics (energy per addition, throughput) from the pre-seed prototype, to verify +85% increase in efficiency and performance.

Table Summary for Investors and Partners

	Arithmetic Processing Core	SHA-256 Compression Engine
Investment Required	**$500, 000 USD**	**$6' 100, 000.00 USD**
Primary Deliverable	Verified RTL core (Prototype) + FPGA benchmarks + simulation models to demonstrate performance and commercial impact.	Full integration of our Arithmetic Core into a Tapeout-ready GDSII File Stream for a Bitcoin mining System-on-Chip.
Delivery time	**6 months**	**10-12 months**
Industrial Applicability	• AI accelerators • Digital Signal Processing • Cryptography and Security • Computer Graphics	Blockchain and Bitcoin Mining
Benefit, broad overview	This package—verified RTL, simulation models, and performance data—is an immediately licensable asset for semiconductor companies. It proves our 30-40% efficiency gains and positions us for a larger Series A.	Our architecture is expected to deliver a meaningful performance and efficiency advantage over existing market solutions, positioning us to capture a significant share of a rapidly expanding market opportunity estimated at +$60 Billion USD.
Business model	*Licensing Arithmetic Core:* • Upfront Licensing Fees • Royalties	*Mining Bitcoin:* • Upfront Licensing Fees • Percentage share of manufacturing yields (in-kind payment) to be employed in Mining
Shareholding	**7% – 10% (SAFE Conversion)**	**15% – 20% (Series A)**
Implied Post-Money Valuation	**$5-7 Million USD**	**$30-40 Million USD**

ALLIANCES
Partners / Clients

We look to work with experts, institutions and businesses

DEVELOPMENT

By working with our clients, we are able to provide custom designed and tailor-fitted critical subunits for digital and analog devices.

Collaborations

Applications and Integration

TEAM

Onboard
Sr. *Engineers*

Research
Math - Physics - CS

INDUSTRY

We are positioned to be a driving froce that will impact almost any sector of science and technology.

Revision of mathematical foundations with efficient operations and other applications.

LEADERSHIP

RESEARCH

Through strategic partnerships and collaborations, we will create a competitive edge.

Middle and Final Customer Satisfaction.

INNOVATION

VALUE

PRODUCTS AND SERVICES

First we focus on a new generation of simple yet powerful processors of unmatched capabilites.

Globally competitive patents for digital and analog systems.

A proposal of new mathematical methods yields results in applied physics, numerical methods, cryptography, data mining, high-performance computing among others.

Mathematically optimized architectures for data science, cryptography, analog and digital devices.

Effective Campaigns

MARKETING AND CUSTOMER EXPERIENCE

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THANK YOU!

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